You can PRINT this pdf file...!!!

Personal Information : Imran Khalid. Roll No. 15DCS0019.
serial No. → 13. Digital Electronics. (DEL-306).
University Polytechnic, Jamia Millia Islamia, N.D-25.

INDEX

S. No	Date	Title	Pg. No.	Remarks

DELTA®
STATIONERY

Scanned by Imran Khalid

20/7/16

Number System

Page no.

Dec. No.	Binary No.	Hexa. Dec. No.	Octal No.
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	8	10
9	1001	9	11
10	1010	A	12
11	1011	B	
12	1100	C	
13	1101	D	
14	1110	E	
15	1111	F	

- $(4237)_{10} = 4000 + 200 + 30 + 7$

$= 4 \times 10^3 + 2 \times 10^2 + 3 \times 10^1 + 7 \times 10^0$

- Conversion from one form to Another form

- $(10110)_2 = (\quad)_{10}$

$= (1 \times 2^4) + (0 \times 2^3) + (1 \times 2^2) + (1 \times 2^1) + (0 \times 2^0)$

$= 16 + 0 + 4 + 2 + 0$

$= (22)_{10}$ Ans

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

- $(22)_{10} \rightarrow (\ )_2$

16	8	4	2	1
1	0	1	1	0

$= (10110)_2$

- $(30)_{10} \rightarrow (\ )_2$

16	8	4	2	1
1	1	1	1	0

$= (11110)_2$

- $(6754)_8 = 6 \times 8^3 + 7 \times 8^2 + 5 \times 8^1 + 4 \times 8^0$

$= 3072 + 448 + 40 + 4$

$= (3564)_{10}$

- $(EB4A)_{16} = 14 \times 16^3 + 11 \times 16^2 + 4 \times 16^1 + 10 \times 16^0$

$= (60234)_{10}$

- $(129.5625)_{10} \rightarrow (\ )_2$

Scanned by Imran Khalid

Page no.

2 | 129	
2 | 64 1	
2 | 32 0	
2 | 16 0	
2 | 8 0	
2 | 4 0	
2 | 2 0	
2 | 1 0 ↑	
1	

$.5625 \times 2 = (1).1250$

$.1250 \times 2 = (0).2500$ ↓

$.2500 \times 2 = (0).5000$

$.5000 \times 2 = (1).0000$

$= (10000001.1001)_2$

- $(657.75)_{10} \rightarrow ()_8$

8 | 657	
8 | 82 1	
8 | 10 2	
8 | 1 2 ↑	
1	

$.75 \times 8 = 6.00$ ↓

$= (1221.6)_8$

- $(657.75)_{10} \rightarrow ()_{16}$

16 | 657	
16 | 41 1	
16 | 2 9	
2 ↑	

$.75 \times 16 = 12\ (E)$

$= (291.E)_{16}$

Scanned by Imran Khalid

$(4429.6)_{10}$

2	4429	
2	2214	1
2	1107	0
2	553	1
2	276	1
2	138	0
2	69	0
2	34	1
2	17	0
2	8	1
2	4	0
2	2	0
	1	0
	1	

$\downarrow$

- $.6 \times 2 = (1).2$
- $.2 \times 2 = (0).4$
- $.4 \times 2 = (0).8$
- $.8 \times 2 = (1).6$
- $.6 \times 2 = (1).2$
- $.2 \times 2 = (0).4$
- $.4 \times 2 = (0).8$

$.100110$

$+\ 1$

$.100111$

$= (10001010011101.10011)_2$

Q. $(.468) \rightarrow$ To hex. Accuracy upto 5 digit.

- $.468 \times 16 = (7).488$
- $.488 \times 16 = (7).808$
- $.808 \times 16 = (12).928 = C$
- $.928 \times 16 = (14).848 = E$
- $.848 \times 16 = (13).568 = D$
- $.568 \times 16 = 9.088$

Scanned by Imran Khalid

• .77CED9

.77CEE1

= (.77CEE)$_{16}$

Ans.

• (764.4)$_8$ to Binary & Hexa.

7 6 4 . 4

111 110 100 100

= (111110100.100)$_2$

0001 1111 0100 . 1000

1 15 4 8

F

= (1F4.8)$_{16}$

Ans.

← Binary Addition

1010 → Augend

1001 → Addend

(10011)$_2$ → sum

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

```
  1011010
+ 11011
(1010101)2
```

```
  0011
+ 1110
 10001
```

- Hexa Addition

```
  1 1
  1AB
+ 67B
 (823)16
```

8+B = 8+11 = 19
= 16+3
18 = 16+2

```
  1 1 1
  ACEF1
+ 16B7D
 (C3A6E)16
```

15+7 = 16+6
1+14+11 = 26 = 16+10
12+7 = 16+3

- Binary substoaction

```
  1010
- 0111
 (0011)2
```

```
  1100 11
- 1001
 (10011)2
```


Scanned by Imran Khalid

Page no.

— Hexa Substraction

$$\begin{array}{r} {}^{1} \\ 8427 \\ AAC \\ \hline (79.7B)_{16} \end{array}$$

Ans.

$7+(1) = 7+16 = 23$

$23 - C = 23 - 12 = 11$

$17 - A = 7$

$16+3 = 19-10$

Q → Substract 22, -15.

→

	Dec No.	sign bit	Magnitude	
	22	0	10110	-A
	-15	1	01111	- B
1's complent	-15	0	10000	- C

Add (A+C) 1 (EAC) 00110 + 1 = $(00111)_2$

Ans.

Q → subtract the following Decmial No. using 8 bit 2's complemont method.

i) -35 from 66.

		128	64	32	16	8	4	2	1	
Decimal No.	sign bit	+	Magnitude							
66	0 (menuhand)	0	1	0	0	0	0	1	0	-A
-35	1 (subtrahand)	0	0	1	0	0	0	1	1	-B
2's complent -35		1	1	0	1	1	1	0	1	-C
Add (A+C)		0	0	0	1	1	1	1	1	

Note:- when menuhand is greater than subtrahand in 2's complemant method a carry is discarded and signbit is not complemented.

When menuend is less than subtrahend in 2's Complement method, the result is re-complemented.

Decimal No.	sign bit	magnitude	
15	0	0000 1111	-A
-22	1	0001 0110	-B
2's complent -22	1	1110 1010	-C
Add (A+C)		1111 1001	
Recomplement		0000 0111	same

Numeric codes

Representing no. within computers and its memory unit by means of electrical signal or magnetising is called numeric coding / codes.

DELTA My NoteBook

Scanned by Imran Khalid

Weighted code

1. BCD - code (Binary coded Decimal)
2. BCO - code (Binary coded octa)
3. BCH - code (Binary coded Hex)

Non-weighted

1. Excess 3 code (XS-3)
2. Gray code

BCD-Code

Dec. No.	8 4 2 1
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Prohibited Code (x)

10 - 1010
11 - 1011
12 - 1100
13 - 1101
14 - 1110
15 - 1111

10 - 0001, 0000
11 - 0001. 0001
12 - 0001. 0010

Q→ 4318 , Add following in BCD code
7678

If there is carryout of '1' or the result of the addition is prohibited code, then add 6 (0110). to LSB, the resulting carry is to be added to next most. significant.

Scanned by Imran Khalid

4318 → 0100 0011 0001 1000

7678 → 0111 0110 0111 1000

1011 1001 1001 0000

+ 0110 0000 0000 0110

0001 0001 1001 1001 0110

1 1 9 9 6

Q → 647 → 0110 0100 0111

492 → 0100 1001 0010

1010 1101 1000

+ 0110 0110 0000

0001 0001 0011 1001

1 1 3 9

Excess 3 code (Xs3)

8 4 2 1 + 3

0000 + 0011 = 0011

0001 + 0011 = 0100

0010 + 0011 = 0101

0011 + 0011 = 0110

0100 + 0011 = 0111

0101 + 0011 = 1000

0110 + 0011 = 1001

0111 + 0011 = 1010

1000 + 0011 = 1011

1001 + 0011 = 1100

Prohibited

0
1
2
14
15

Scanned by Imran Khalid

$(357)_{10} \rightarrow Xs3$

3 5 7

0011 0101 0111

\+ 0011 0011 0011

0110 1000 1010

$(864)_{10} \rightarrow Xs3$

8 6 4

1000 0110 0100

\+ 0011 0011 0011

$(1011\ 1001\ 0111)_{Xs3}$

- **Addition of Xs3**

Note: If there is a no carryout from the four bit group subtract $(0011)_2$ '3' & if there is a carryout then add '3' $(0011)_2$ to sum as well as carry.

3 → 0110 $_{Xs3}$

2 → 0101

1011

-0011

$(1000)_{Xs3}$

Scanned by Imran Khalid

6 → 1001
8 → 1011

0001 0100
+0011 +0011

0100 0111) XS3

1 4

Gray Code

Dec No.	Binary No.	Gray code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010

Convert to Gray Code

1 0 1 1 (L→R)

1 1 1 0 (carry discarded)

1 0 0 1 0 1 1

1 1 0 1 1 1 0

27/7/2016

Page no.

Convert Gray Code to Binary

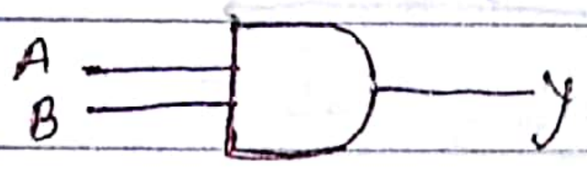
1 0 1 1

↓ + ↗ + ↗ + ↗

1 1 0 1 (All cary Discarded)

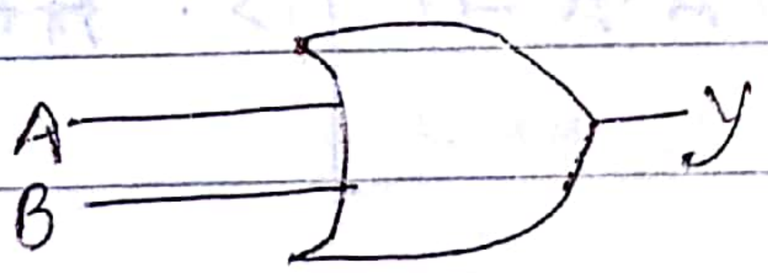
• Logic Gates & Boolean Algebra

→ **AND Gate**



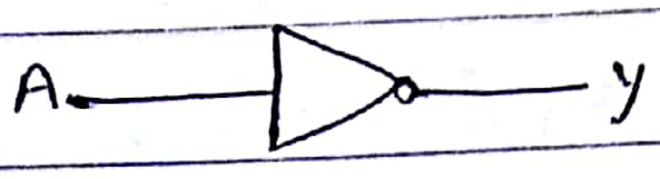
A	B	Y = A·B
0	0	0
0	1	0
1	0	0
1	1	1

→ **OR Gate**



A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

→ **NOT Gate**

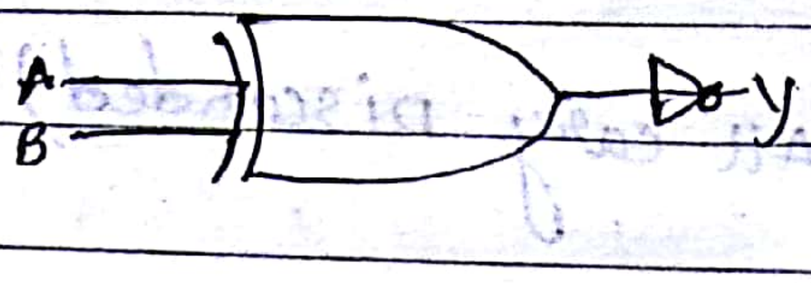


A	Y = $\bar{A}$
0	1
1	0

Scanned by Imran Khalid

Page no.

Exclusive NOR Gate



Truth Table

A	B	$Y = A+B$	$Y = \overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Basic law

1. $\bar{0} = 1$
2. $\bar{1} = 0$
3. $A = 0$, $\bar{A} = 1$
4. $A = 1$, $\bar{A} = 0$
5. $\bar{\bar{A}} = A$

AND Law

6. $A \cdot 0 = 0$
7. $A \cdot 1 = A$
8. $A \cdot A = A$
9. $A \cdot \bar{A} = 0$

OR Laws

10. $A + 1 = 1$
11. $A + 0 = A$
12. $A + A = A$
13. $A + \bar{A} = 1$

Commulative Laws

14. $A + B = B + A$
15. $A \cdot B = B \cdot A$

Associative Laws

16. $A + (B+C) = (A+B) + C$
17. $(A+B) + (C+D) = A+B+C+D$
18. $A \cdot (BC) = (A \cdot B) \cdot C$

Distributive law

19. $A(B+C) = (A \cdot B) + (A \cdot C)$
20. $A + (B \cdot C) = (A+B) \cdot (A+C)$
21. $A + (\bar{A} \cdot B) = A + B$

DELTA My NoteBook

Scanned by Imran Khalid

Prove $A+(B.C)=(A+B).(A+C)$

$L.H.S = A+(B.C)$

$= A.1+(B.C)$ — L 7

$= A(1+B)+(B.C)$ — L 10

$= A+AB+(B.C)$

$= A.1+AB+BC$

$= A(1+C)+AB+BC$ — L 10

$= A+AC+AB+BC$

$= A.A+AC+AB+BC$

$= A(A+C)+B(A+C)$

$= (A+B).(A+C) = R.H.S$

Prove $A+(\bar{A}.B)=A+B$

$L.H.S = A+(\bar{A}.B)$

$= A1+(\bar{A}.B)$

$= A(1+B)+(\bar{A}.B)$

$= A+AB+\bar{A}B$

$= A+B(A+\bar{A})$

$= (A+B).1$

$= A+B = R.H.S$

simplify : $(A+\bar{B}).C+(B+\bar{C}).A+\bar{A}.B = A+B+C$

$L.H.S = AC+\bar{B}C+AB+A\bar{C}+\bar{A}.B$

$= (AC+A\bar{C})+(AB+\bar{A}.B)+\bar{B}.C$

$= A(C+\bar{C})+B(A+\bar{A})+\bar{B}.C$

$= A+B+\bar{B}C$

$= A+B+B(1+C)+\bar{B}C$

$= A+B+C(B+\bar{B})$

$= A+B+C = R.H.S$

DELTA My NoteBook

Scanned by Imran Khalid

simplify: $(AB+C)(AB+D) = AB+CD$

L.H.S $= AB.AB + ABD + CAB + CD$

$= AB(1+C) + ABD + CD$

$= AB + ABC + CD$

$= AB(1+D) + CD$

$= AB + CD = RHS$

simplify the following expression and show min. gate implementation.

$Y = A.B.\bar{C}.\bar{D} + \bar{A}B\bar{C}\bar{D} + B\bar{C}D$

$= \bar{C}\bar{D}(AB + \bar{A}B) + B\bar{C}D$

$= B\bar{C}\bar{D}(A + \bar{A}) + B\bar{C}D$

$= B\bar{C}\bar{D}.1 + B\bar{C}D$

$= B\bar{C}(D+\bar{D})$

$= B\bar{C}.$

Simplify: prove $A(\bar{A}+C).(\bar{A}B+\bar{C}) = 0$

$= (A\bar{A} + AC).(\bar{A}B+\bar{C})$

$= AC.(\bar{A}B+\bar{C})$

$= A\bar{A}BC + AC\bar{C}$

$= (0).BC + A(0)$

$= 0$

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

De-morgans Theorem

1. The complement of a sum equalls the product of the complement.

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

2. The complement of a product equalls the sum of the complement

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

Procedure carried out for the implementation of the two laws.

1. Complement the entire given expression

$$\overline{A+BC} = \overline{\overline{A+BC}}$$

2. Change all the AND's to OR's & OR's to AND's

$$\overline{\overline{A+BC}} = A+BC$$
$$= A \cdot (B+C)$$

3. Complement all the individual variable

$$\bar{A} \cdot (\bar{B}+\bar{C})$$

Q → $(\bar{A}+B+\bar{C})(\bar{A}+B+C)$ simplify.

Ans → $\overline{(\bar{A}+B+\bar{C})(\bar{A}+B+C)}$ $\quad \bar{\bar{A}} = A$

$= (\bar{A}+B+\bar{C})(\bar{A}+B+C)$

$= (\bar{A} \cdot B \cdot \bar{C}) + (\bar{A} B C)$

$= (\bar{\bar{A}} \cdot \bar{B}\,\bar{\bar{C}}) + (\bar{\bar{A}}\,\bar{B}\,\bar{\bar{C}})$

$= (A\bar{B}C) + (A\bar{B}\bar{C})$

$= A\bar{B}(C+\bar{C}) = A\bar{B}$

DELTA My NoteBook

Scanned by Imran Khalid

Q → simplify : $\overline{AB+BC+CA} = \bar{A}.\bar{B} + \bar{B}.\bar{C} + \bar{A}.\bar{C}$

Ans → L.H.S = $\overline{AB+BC+CA}$

$= \overline{AB} . \overline{(BC+CA)}$

$= \overline{AB} . \overline{[C(B+A)]}$

$= (\bar{A}+\bar{B}) . [\bar{C} + (\bar{B}\bar{A})]$

$= (\bar{A}+\bar{B}) . [\bar{C} + \bar{B}\bar{A}]$

$= (\bar{A}+\bar{B})$

$= \bar{A}\bar{C} + \bar{A}\bar{A}\bar{B} + \bar{B}.\bar{C} + \bar{B}\bar{B}\bar{A}$

$= \bar{A}.\bar{C} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{B}$

$= \bar{A}\bar{B} + \bar{B}.\bar{C} + \bar{A}\bar{C}$

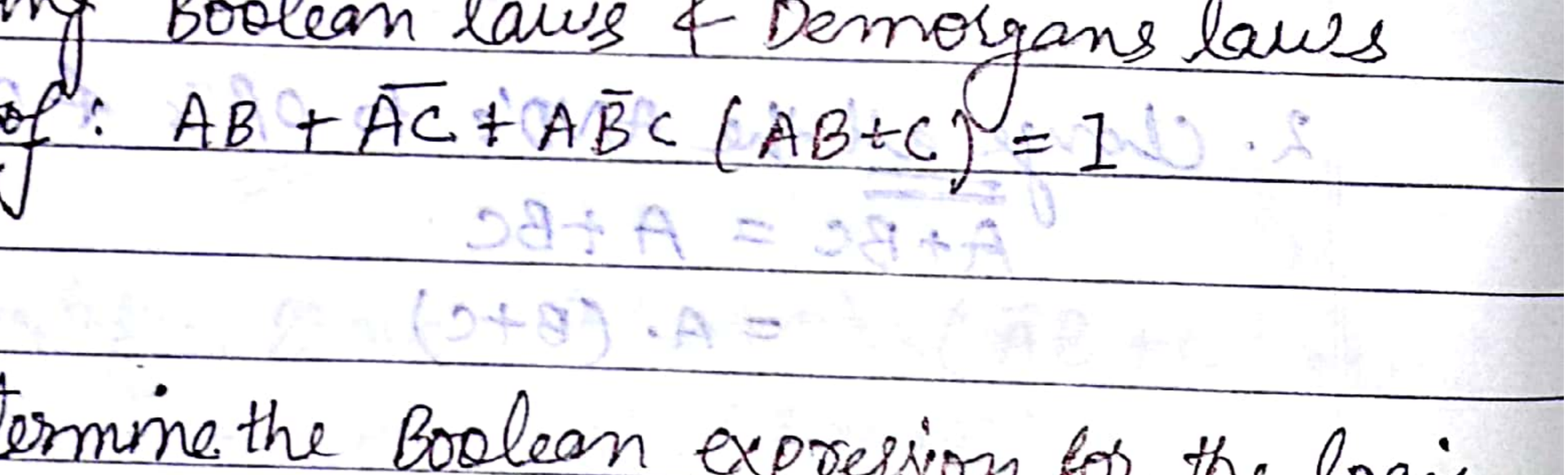
= R.H.S

Ans.

Q → Using Boolean laws & Demorgans laws

proof : $AB + \bar{A}C + A\bar{B}C\,(AB+C) = 1$

Q → Determine the Boolean expression for the logic ckt. as shown below. simplify the output so obtained then Re Draw logic ckt.



Scanned by Imran Khalid

03/8/2018

Page no.

$$y = AC.\overline{(AB+\bar{C})}$$

$$= AC.\overline{\bar{A}B+\bar{C}}$$

$$= AC.\overline{(A+B).\bar{C}}$$

$$= AC.[\bar{A}+\bar{B}).\bar{\bar{C}}]$$

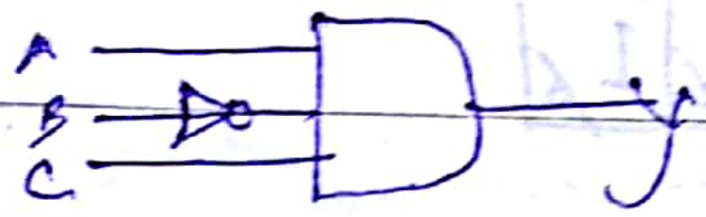
$$= AC.(\bar{A}+\bar{B}).C$$

$$= AC.C(A+\bar{B})$$

$$= AC(A+\bar{B})$$

$$= A\bar{A}C + AC\bar{B}$$

$$= A\bar{B}C$$



Karnaugh Map

Minterms: The Boolean function can be expressed as the sum of products of all the variables within the system.

Let $y = A+B$

$= A(B+\bar{B}) + B(A+\bar{A})$

$= AB + A\bar{B} + AB + \bar{A}B$

$y = AB + A\bar{B} + \bar{A}B$,

minterms

Scanned by CamScanner

If we assign a '0' for NOTE term and " " '1' remote.

$$y = A\bar{B} + A\bar{B} + \bar{A}B$$
$$= 11 + 10 + 01$$
$$= 3 + 2 + 1$$
$$y = \Sigma m\,(1,2,3)$$

A \ B	0	1
0	0 (0)	1 (1)
1	1 (2)	1 (3)

$$y = \bar{A}\bar{B} + \bar{A}B + A\bar{B} + AB$$

Q → Draw the Karnaugh map for the equation
$y = \Sigma m\,(1,5,7)$.

Max. countable No. 7.
Binary eq. of 7 = 111.
(n) No. of variable = 3
No. of Square = $2^n = 2^3 = 8$

A \ BC	00	01	11	10
0	0 (0)	1 (1)	0 (3)	0 (2)
1	0 (4)	1 (5)	1 (7)	0 (6)

Scanned by Imran Khalid

Page no.

Q → Draw the K-map for the equation

$$y = ABC + A\bar{B}C + AB\bar{C}$$

$$y = 111 + 101 + 100$$
$$= 7 + 5 + 4$$
$$y = \Sigma m\,(7, 5, 4).$$

Max. combination = 7

Binary eq. of 7 = 111

No. of square $2^m = 2^3 = 8$

A \ BC	00	01	11	10
0	0 (0)	0 (1)	0 (3)	0 (2)
1	1 (4)	1 (5)	1 (7)	0 (6)

Q → Draw the K-Map for the equation

$$y = \Sigma m\,(1, 2, 3, 4, 5, 9, 11, 12, 13, 15)$$

Max. countable No. = 15

Binary eq. of 15 = 1111

No. of square = $2^4 = 16$

AB \ CD	00	01	11	10
00	0 (0)	1 (1)	1 (3)	1 (2)
01	1 (4)	1 (5)	0 (7)	0 (6)
11	1 (12)	1 (13)	1 (15)	0 (14)
10	0 (8)	1 (9)	1 (11)	0 (10)

(Map Reduction Technique)

DELTA My NoteBook

Scanned by Imran Khalid

Q → Draw the K-Map for the equation

$Y = \Sigma m (0, 2, 3, 4, 5, 7)$

Max. Countable No. 7 (111)

No. of square $= 2^3 = 8$

A \ BC	00	01	11	10
0	1 (0)	0 (1)	1 (3)	1 (2)
1	1 (4)	1 (5)	1 (7)	0 (6)

Pair 1 = $\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$

$= \bar{B}\bar{C}(A + \bar{A})$

$= \bar{B}\bar{C}$

Pair 2 = $\bar{A}\bar{B}C + A\bar{B}C$

$= A\bar{B}(C + \bar{C})$

$= A\bar{B}$

Pair 3 = $A\bar{B}C + ABC$

$= AC(B + \bar{B})$

$= AC$

Pair 4 = $\bar{A}BC + ABC$

$= BC(A + \bar{A})$

$= BC$

Pair 5 = $\bar{A}BC + \bar{A}B\bar{C}$

$= \bar{A}B(C + \bar{C})$

$= \bar{A}B$

DELTA My NoteBook

Scanned by Imran Khalid

$\bar{B}\bar{C} + AC + \bar{A}B$

Page no.

$$y = \bar{B}\bar{C} + A\bar{B} + AC + BC + \bar{A}B$$

	A \ BC	00	01	11	10
0		1	0	1	1
1		1	1	1	0

Pair 1 $= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}$

$= \bar{A}\bar{C}(B + \bar{B})$

$= \bar{A}\bar{C}$

Pair 2 $= A\bar{B}\bar{C} + A\bar{B}C$

$= A\bar{B}$

Pair 3 $= \bar{A}BC + ABC$

$= BC$

~~Pair 4 =~~

$$y = \bar{A}\bar{C} + A\bar{B} + BC$$

(SOP)

DELTA My NoteBook

Scanned by Imran Khalid

SOP :-

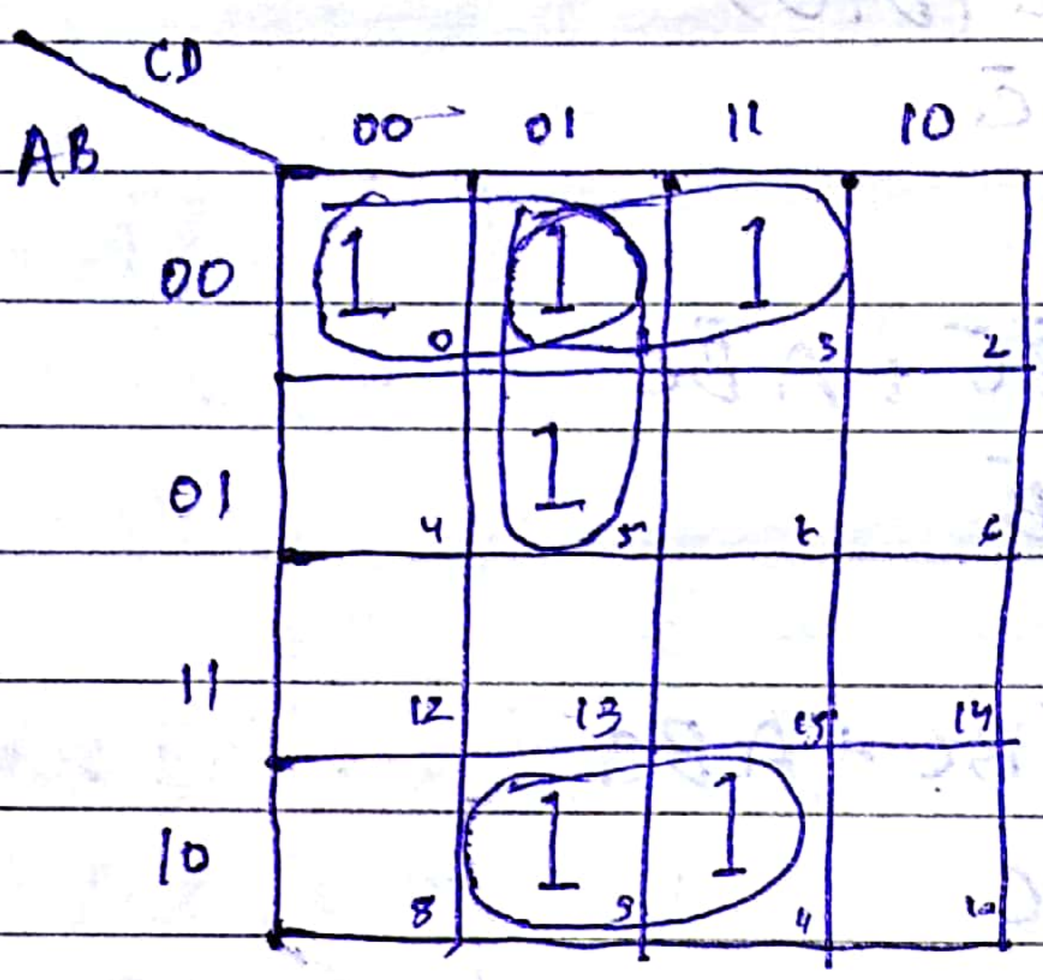
Implement the following using least no. of gates.

$$Y = \Sigma m (0, 1, 3, 5, 9, 11)$$

Max. countable no. = 91

Binary of 9 = 1001

square = $2^4 = 16$



Pair 1 = $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$

$= \bar{A}\bar{B}\bar{C}$

Pair 2 = $\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD$

$= \bar{A}\bar{B}D$

Pair 3 = $\bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D$

$= \bar{A}\bar{C}D$

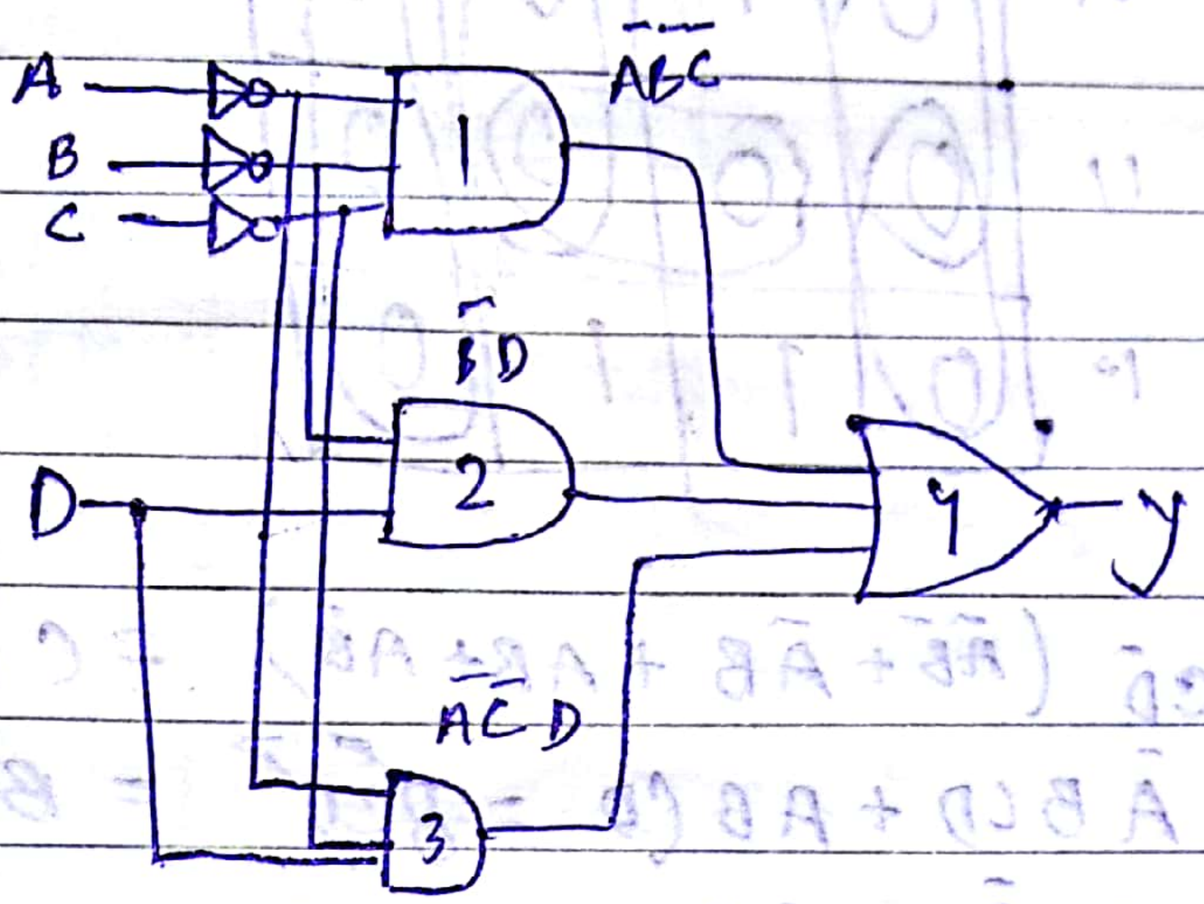
Pair 4 = $A\bar{B}\bar{C}D + A\bar{B}CD$

$= A\bar{B}D$

Scanned by Imran Khalid

$$y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}D + \bar{A}\bar{C}D + A\bar{B}D$$

$$= \bar{B}D + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{C}D$$



POS:-

Implement the following using least no. of gates. Find the POS of the following.

$$y = \Sigma_M (0, 1, 3, 5, 9, 11)$$

- Combine the zeroes into 2^n
- Read the zeroes from the map & record the variables.
- Changes the AND's to OR's. and complement each variable.
- Find the product of these sums.

Scanned by Imran Khalid

AB \ CD	00	01	11	10
00	1	1	1	0
01	0	1	0	0
11	0	0	0	0
10	0	1	1	0

$Y_1 = C\bar{D}\,(\bar{A}\bar{B} + \bar{A}B + AB + A\bar{B}) = C\bar{D}$

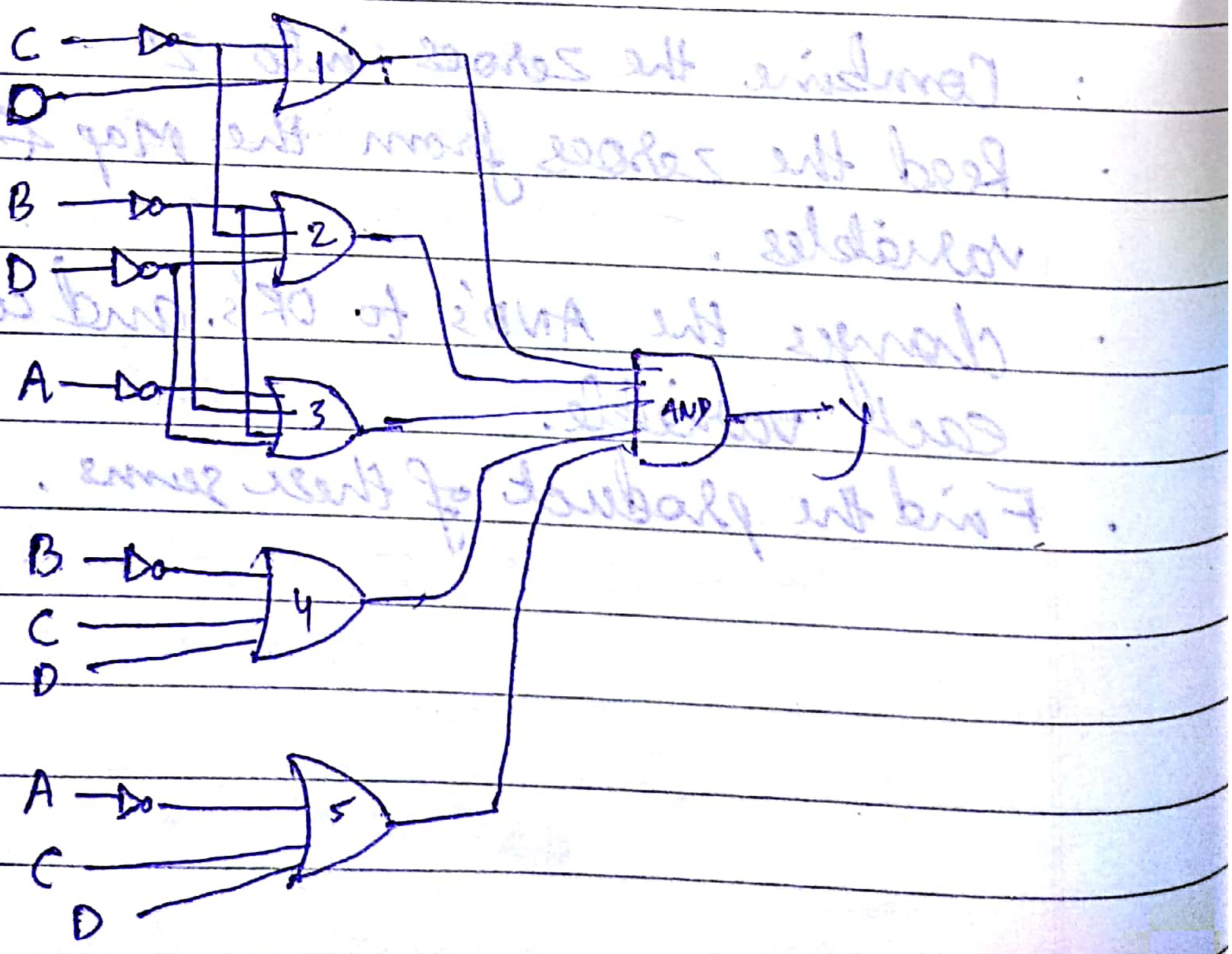
$Y_2 = \bar{A}BCD + AB(\bar{C}D = B\bar{C}D = BCD$

$Y_3 = AB\bar{C}D + ABCD = ABD$

$Y_4 = \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} = B\bar{C}\bar{D}$

$Y_5 = AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} = A\bar{C}\bar{D}$

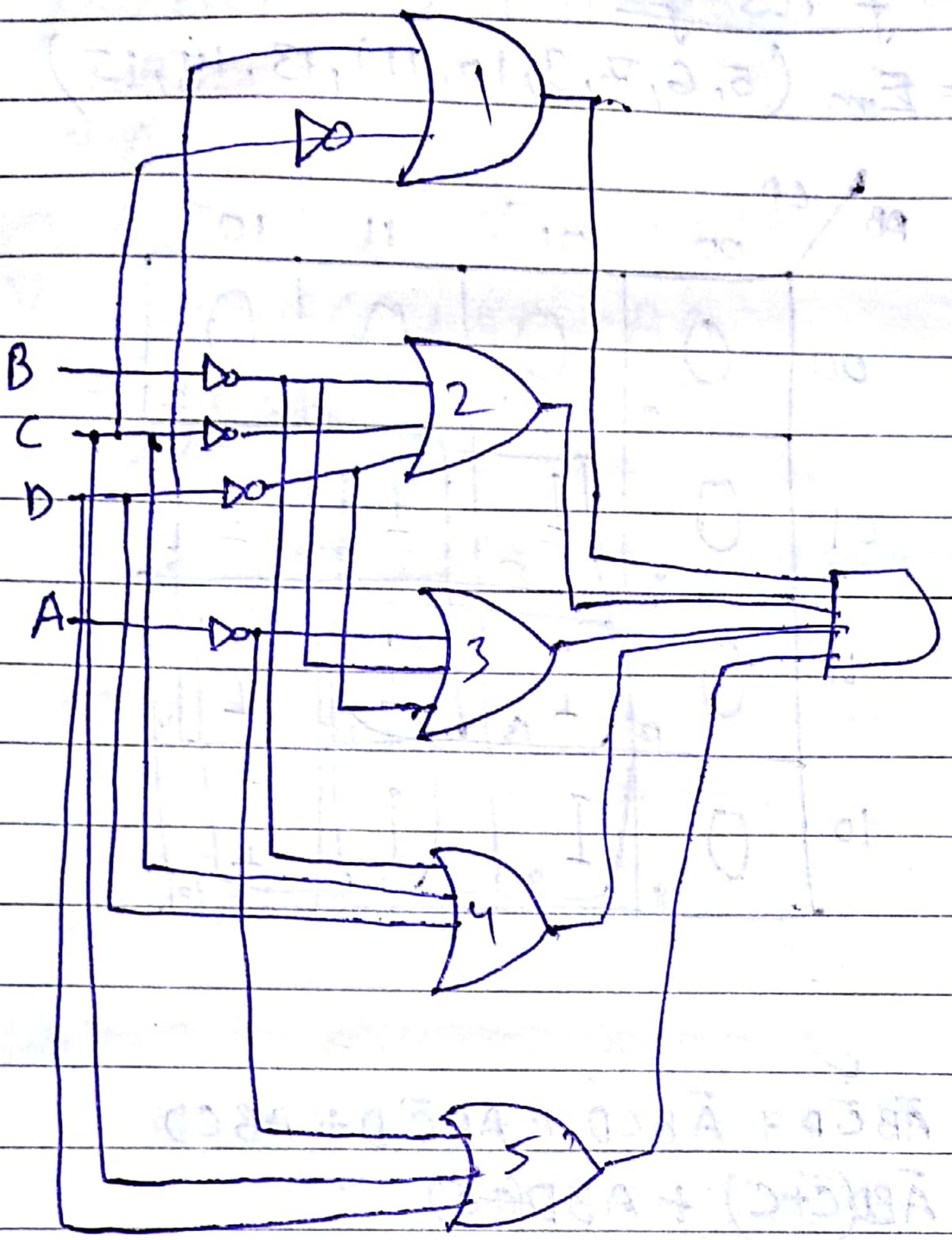
$Y = (\bar{C} + \bar{D}) \cdot (B + \bar{C} + \bar{D}) \cdot (\bar{A} + \bar{B} + \bar{D}) \cdot (\bar{B} + C + D) \cdot (\bar{A} + C + D)$



Scanned by Imran Khalid

04/08/2016

Page no.



Q → Find POS & SOP form of
$Y = \Sigma m (0,1,3,5,7,8,9,13,15)$.

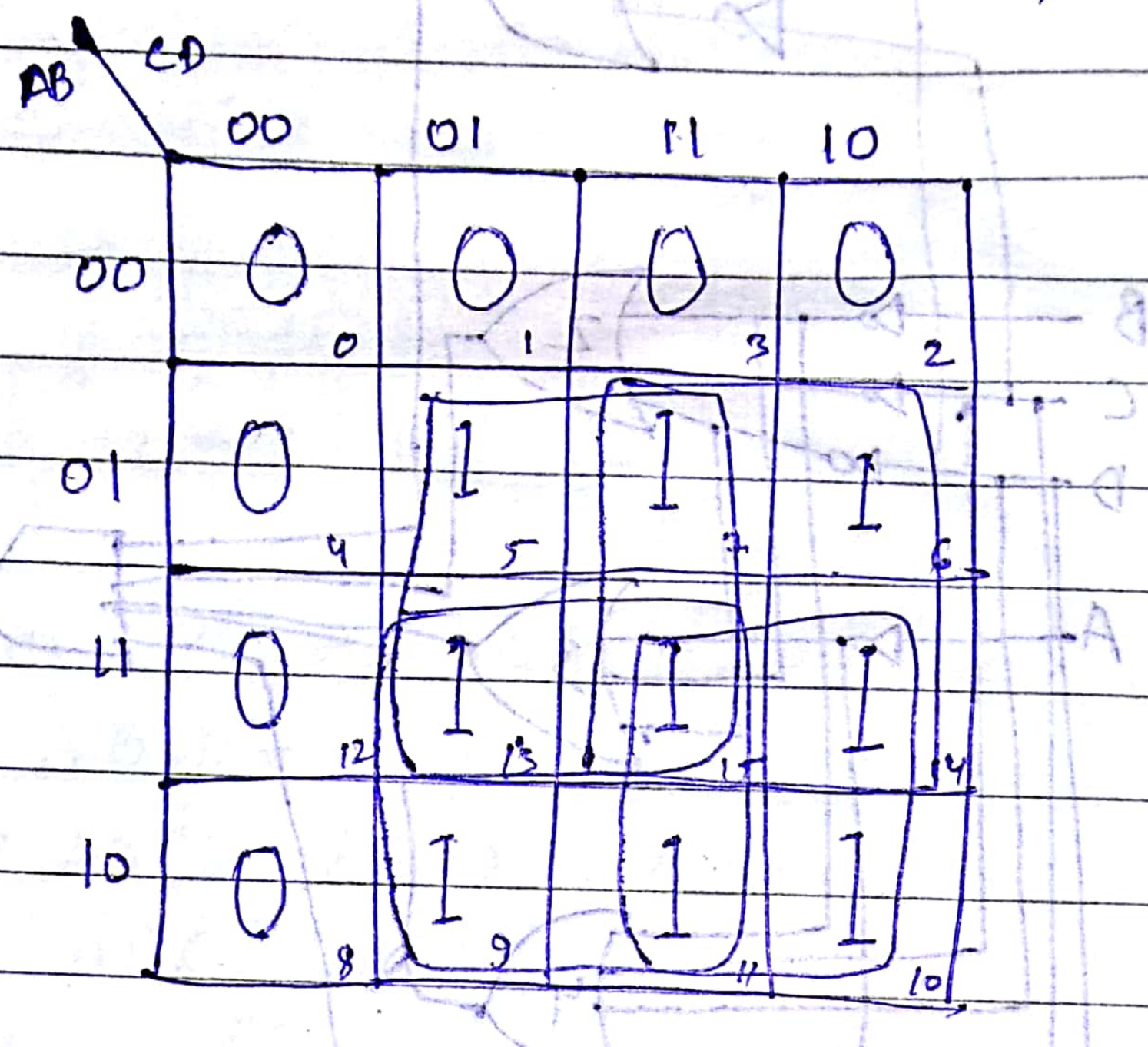
Scanned by Imran Khalid

08/04/2016

Page no.

SOP & POS of

$Y = Em(5, 6, 7, 9, 10, 11), 13, 14, 15)$



$Y_1 = \bar{A}B\bar{C}D + \bar{A}BCD + AB\bar{C}D + ABCD$

$= \bar{A}BD(\bar{C}+C) + ABD(\bar{C}+C)$

$= \bar{A}BD + ABD$

$= BD$

$Y_2 = \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + AB\bar{C}D + ABC\bar{D}$

$= \bar{A}BC + ABC$

$= BC$

$Y_3 = AB\bar{C}D + ABCD + A\bar{B}\bar{C}D + A\bar{B}CD$

$= ABD + A\bar{B}D$

$= AD$

Scanned by Imran Khalid

$$Y_2 = ABCD + ABC\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D}$$

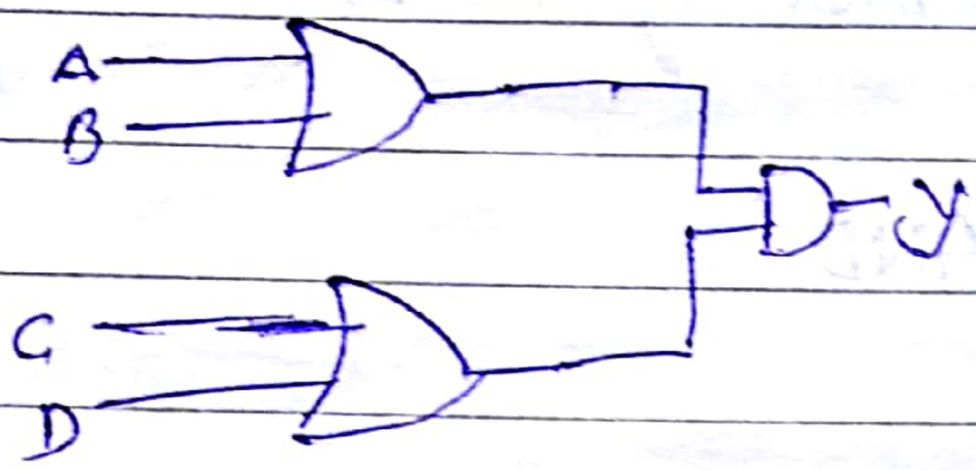
$$= ABC + A\bar{B}C$$

$$= AC$$

$$Y = BD + BC + AD + AC$$

$$= B(C+D) + A(C+D)$$

$$= (B+A).(C+D)$$

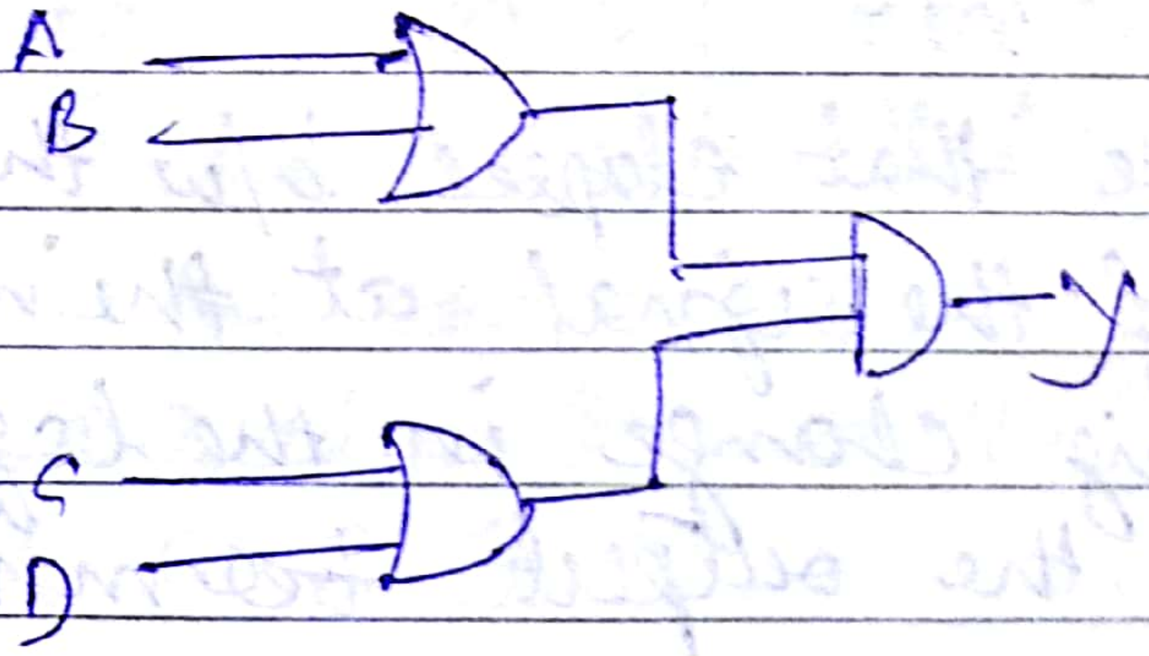


POS:-

$$Y_1 = \overline{A\bar{B}} = \bar{A}+B = \overline{\bar{A}+B} = A+\bar{B}$$

$$Y_2 = \overline{\bar{C}\bar{D}} = \bar{C}+D = \overline{C+\bar{D}}$$

$$Y = (A+B).(C+D)$$



Scanned by Imran Khalid

Logic families

1. R.T.L ×
2. D.T.L → Diodle Transistor logic - NAND
3. T.T.L " " " (faster)
4. Schottky T.T.L " "
5. E.C.L → emitter coupled logic = OR/NOR
6. I^2L → Integrated injection logic → "
7. CMOS → complementry metal oxide semicontor.

D.T.L → NAND

Characteristics of logic families

1. **Logic levels**

L.L are values of voltages corrocponding to logic state. (0, 1)

2. **speed**

It is the time that elapses b/w the application of the signal at the input and resulting change in the logic state, at the output terminal.

3. **propagation delay time**

It is the average transition delay time for the signal to propogate from

DELTA MyNoteBook

Scanned by Imran Khalid

input to output when the binary signal changes its value.

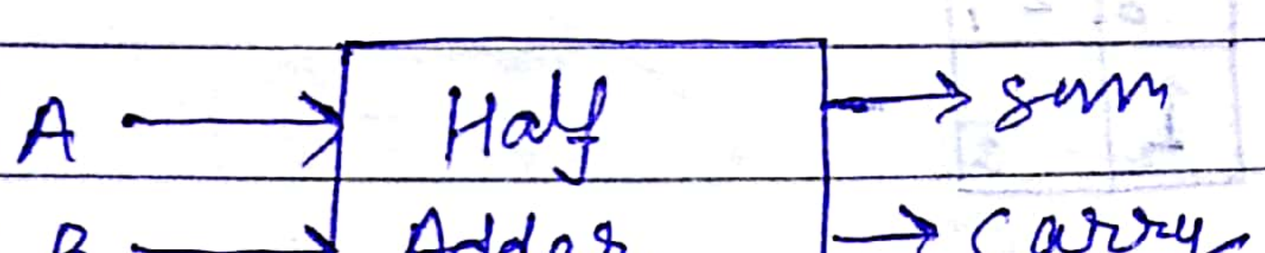
Fan in and fan out

It is the max. no. of gates that the output of any logic gate can drive without getting its output. The limit is called fanout.

It is the max. no. of input which a logic gate can with stand, without getting its logic level shifting. The limit is called fan-in.

Half Adder

It is a logic ckt which can add to binary no. at a time to produce to two bit data of which one is the submitted & the other is the carry. The addition is carried out with the help of XOR & AND Gate.



Block Digram

Scanned by Imran Khalid

T.T

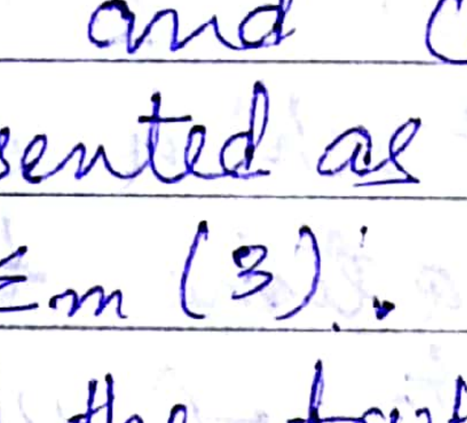
Page no.

Dec	A	B	sum (S)	carry (C)
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1

Design

looking into the tooth table be find the decimal values for which the sum 'S' is high are (1,2) and decimal values for which the carry 'C' is high (3). Therefore, the sum and carry can be represented as $S = \Sigma m(1,2)$ & $C = \Sigma m(3)$.

Using the tooth table we can draw the K-Map and find the equation for the sum & carryout.



Sum $y_1 = \bar{A}B + A\bar{B}$ =

DELTA My NoteBook

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

9/8/14

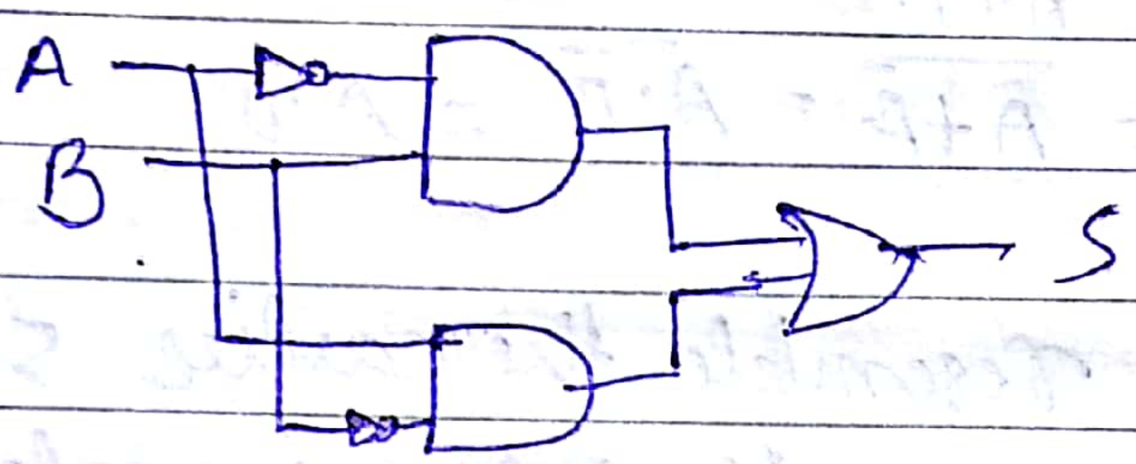
Page no.

A \ B_0	0	1
0	0	1
1	2	1_3

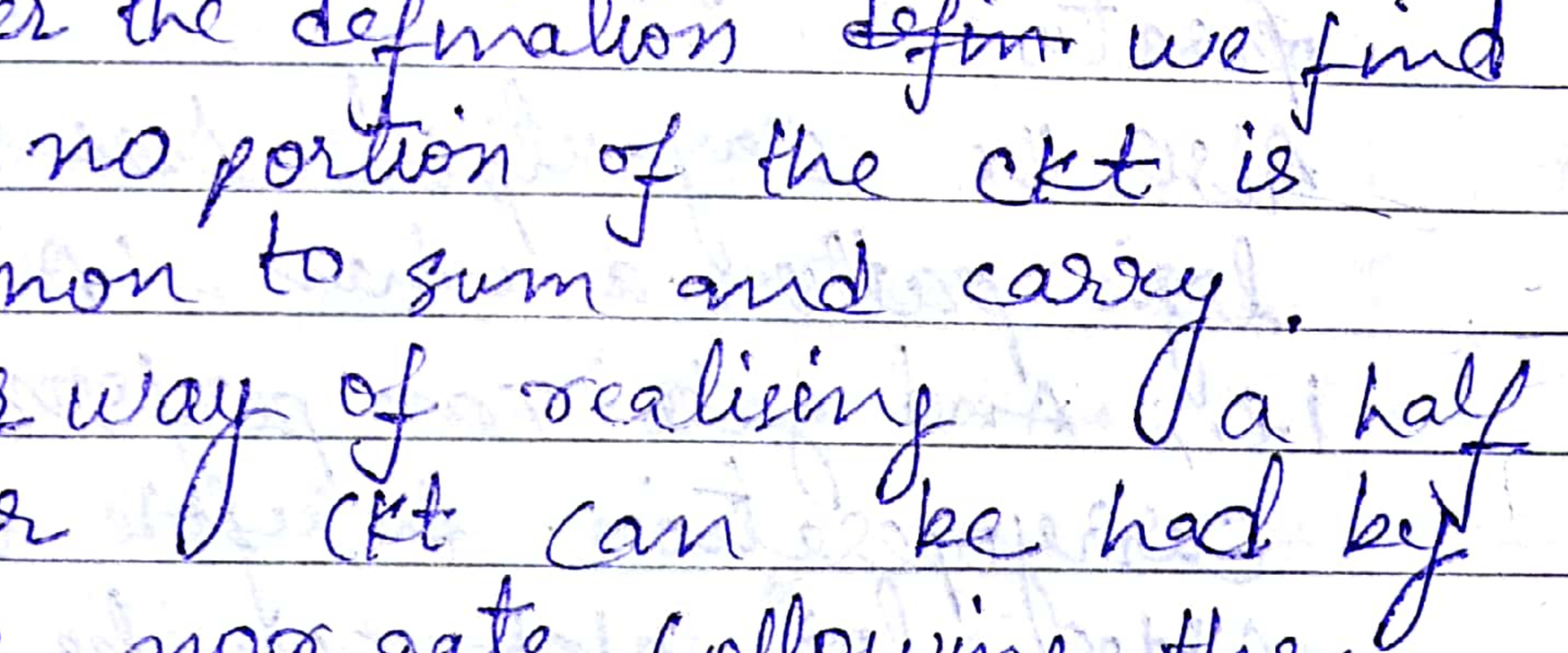
(carry)

$C = Y = AB$

Using the above equation the following logic circuit can be realised.



As per the ~~defin~~ definiation we find that no portion of the ckt is common to sum and carry. Better way of realising a half adder ckt can be had by using nor gate following the definiation



DELTA My NoteBook

Scanned by Imran Khalid

The equation governing above ckt are simplifying the above equation

$$S = \overline{(\overline{A+B})} + \overline{(\overline{\bar{A}+\bar{B}})}$$

$$= \overline{(\overline{A+B})} \cdot \overline{\bar{A}+\bar{B}}$$

$$= (A+B) \cdot (\bar{A}+\bar{B})$$

$$= A\bar{A} + A\bar{B} + B\bar{A} + B\bar{B}$$

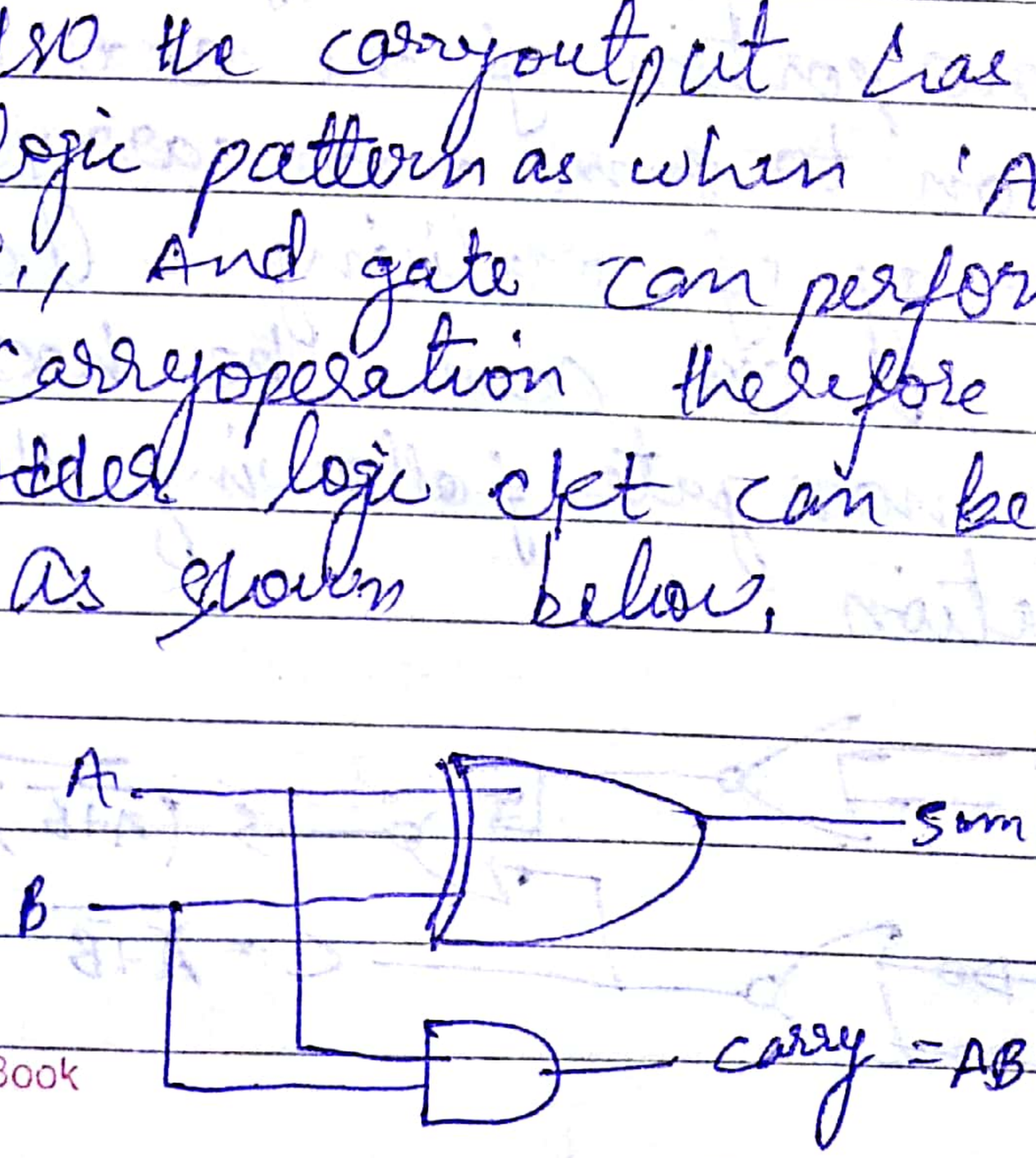
$$= A\bar{B} + B\bar{A}$$

$$S = A+B$$

$$C = \overline{\bar{A}+\bar{B}} = \bar{A} \cdot \bar{\bar{B}} = A \cdot B$$

clearly resemble the earlier sections found from K-MAP. We also find that the some output has same logic pattern as when A is X-ORed B that is XOR gate can represent some operation

Also the carryoutput has the same logic pattern as when 'A' is ANDed B. i.e., And gate can perform the carryoperation therefore the half added logic ckt can be found. As shown below,



DELTA My NoteBook

Scanned by Imran Khalid

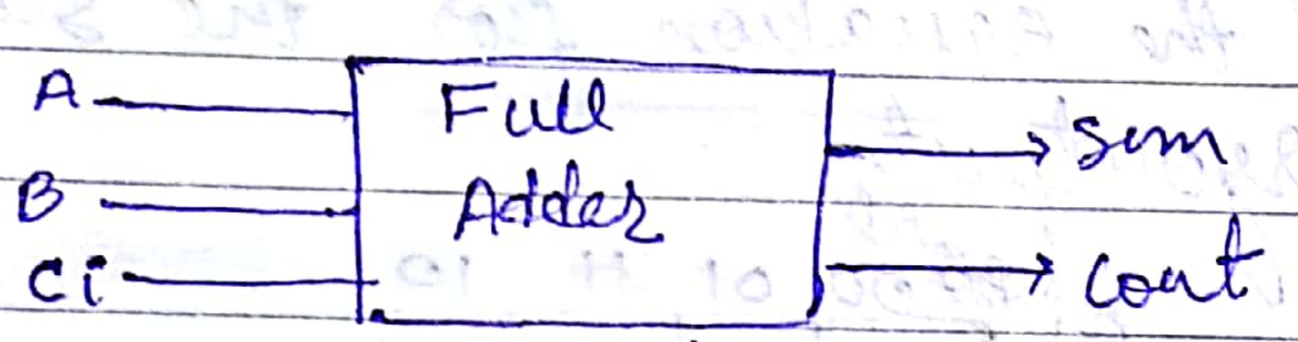
10/8/2016

Page no.

Full Adder

T.T

Dec.	A	B	Carry IN (Ci)	Sum S	Carry out (C)
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1



Block diagram

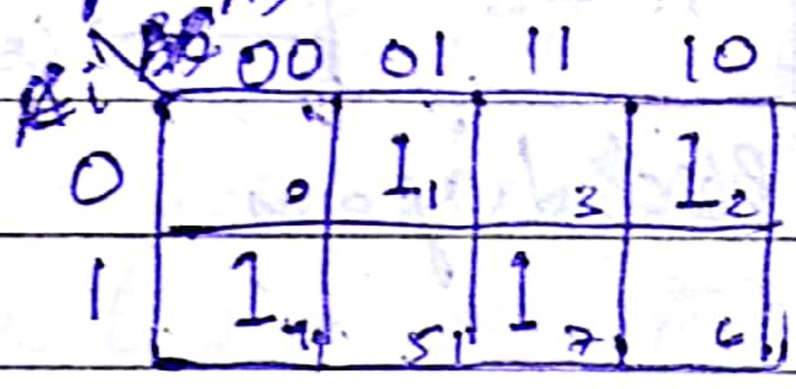
It is a logic ckt which can act three binary digits at a time to produce a bit data of which one is the sum bit and other is the carryout bit. The bits A & B which are to be added come from two registers and the third bit come from the carry generated by the previous addition the addition is carried out with the help of two half adders & OR gates

Scanned by Imran Khalid

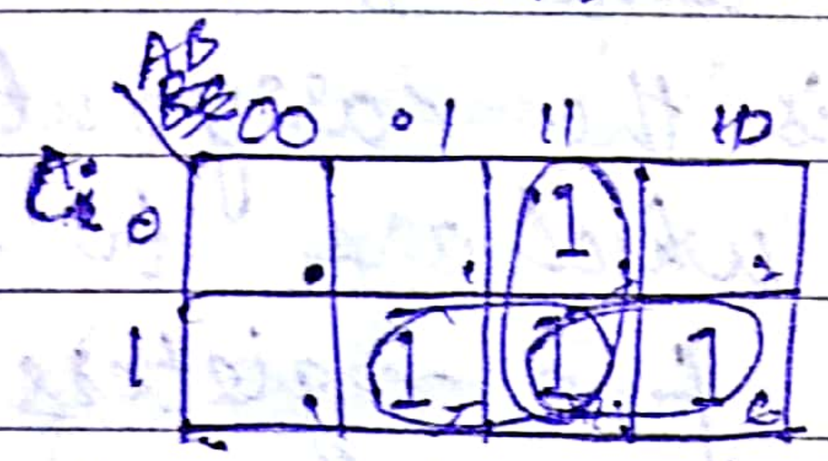
Page no.

Design procedure

looking into the truth table we find the values for which the sum (S) is high are $S = \Sigma m(1,2,4,7)$ and the decimal values for which the carryout is high are (3,5,6,7). Therefore, the sum & carry can be represented as $S = \Sigma m(1,2,4,7)$ and $Co = \Sigma m(3,5,6,7)$. Using the truth table we can draw the K-map & find the equation for the sum and carryoutput.



$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{C_i}BC + \bar{C_i}B\bar{C} + C_iB\bar{C} + C_iBC$$



$$C_o = \bar{A}BC + ABC + A\bar{B}C + ABC + ABC + AB$$
$$= BC + AC + AB$$
$$= BC + AC_o + C_oB$$

Scanned by Imran Khalid

10/08/2016

Page no.

$$S = A\bar{B}\bar{C}i + A\bar{B}C\bar{i} + A\bar{B}\bar{C}\bar{i} + ABCi$$

$$= (\bar{A}B + A\bar{B})C\bar{i} + (A\bar{B} + AB)Ci$$

$$= (A \oplus B)C\bar{i} + (\overline{A \oplus B})Ci$$

$$A \oplus B = \bar{A}B + A\bar{B}$$

$$= \overline{\bar{A}B + A\bar{B}}$$

$$= (\bar{A} + B).(\bar{A} + \bar{B})$$

$$= \bar{A}A + \bar{A}\bar{B} + BA + B\bar{B}$$

Let $A \oplus B = x$

Then

$$= xC\bar{i} + \bar{x}Ci = (x \oplus Ci)$$

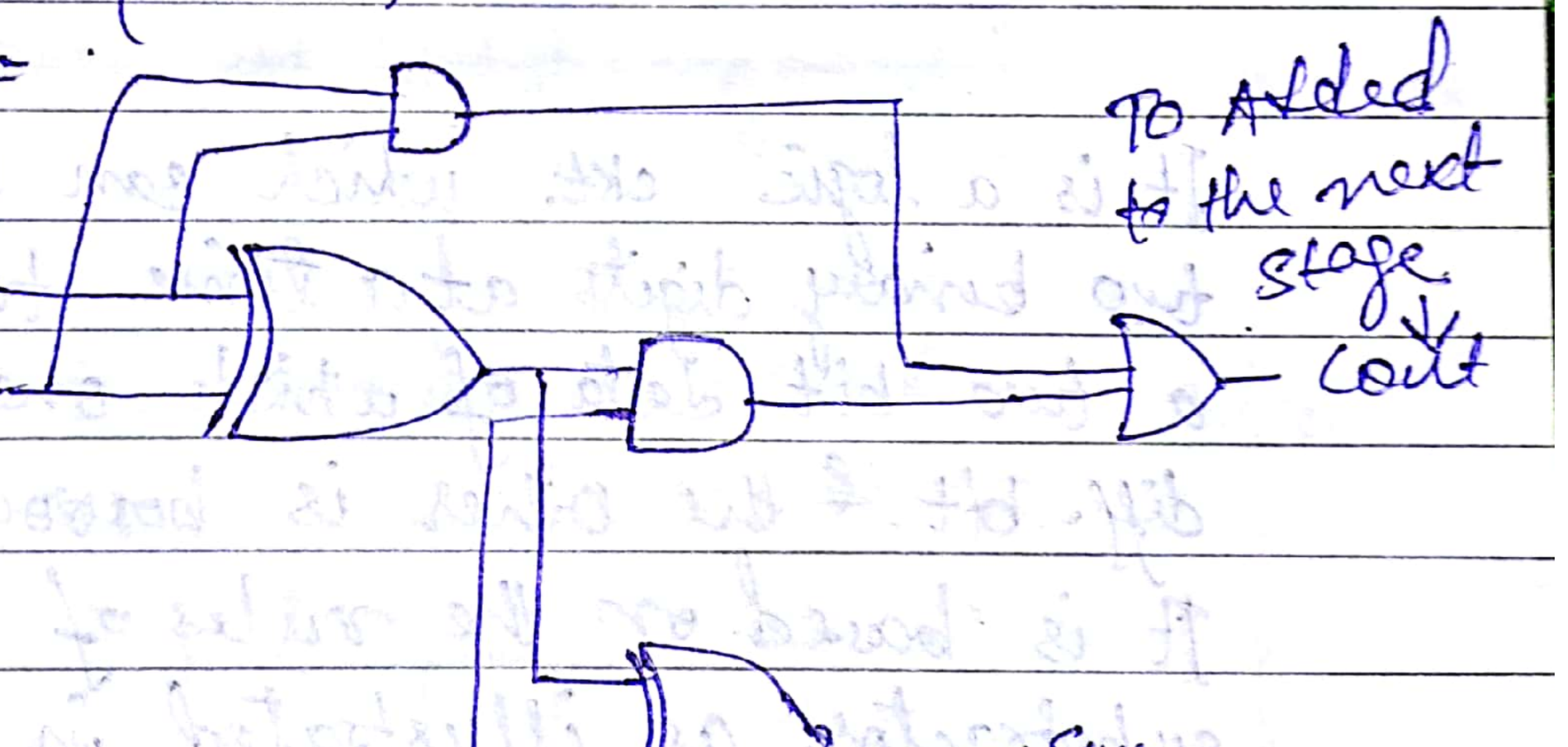
$$S = A \oplus B \oplus Ci$$

$$C_o = \bar{C}_o AB + C_o + C_o\bar{A}B + C_oBA + C_o\bar{A}\bar{B}$$

$$= (\bar{A}B + A\bar{B})Ci + (Ci + C\bar{i})AB$$

$$C_o = (A \oplus B) \cdot Ci + AB$$

=



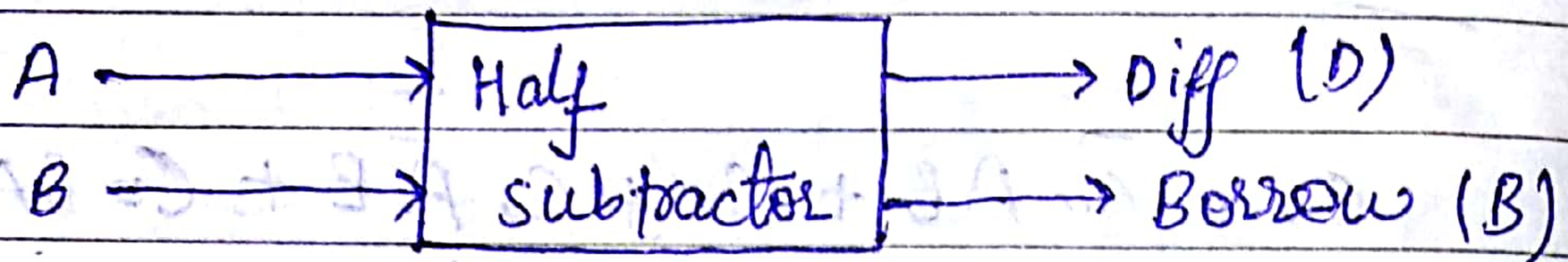
DELTA My NoteBook

Scanned by Imran Khalid

Half subtractor

T.T

Dec.	A	B	Difference (Di)	Borrow (Bi)
0	0	0	0	0
1	0	1	1	1
2	1	0	1	0
3	1	1	0	0



Block diagram

It is a logic ckt. which can substract two binary digits at a time to produce a two bit data of which one is the diff. bit & the other is borrow bit. It is based on the rules of binary substractor as illustrated in the truth table. The Diff. column show the same logic pattern as when $A \oplus B$. Therefore XOR gate can be used to get the diff. of ~~true~~ two bits. The borrow output is obtained by ANDing $\bar{A} \cdot B$

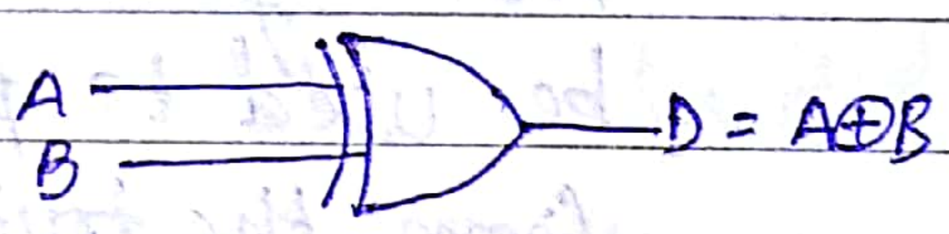
DELTA My NoteBook

Scanned by Imran Khalid

Design procedure

Looking into the Truth table we find the decimal values for which decimal B is high are 1, 2, the borrow B is high is 1. Therefore the Diff. & borrow can be represented as $D = \Sigma m(1,2)$, $B = \Sigma m(1)$. Using the truth table we can the K-Map and find the equation for the Diff. & borrow.

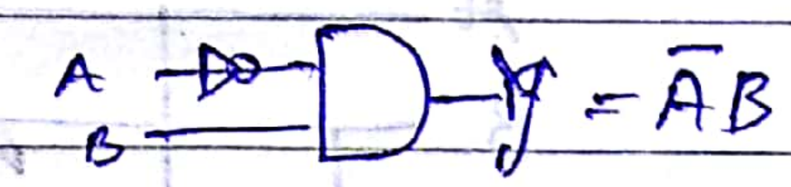
A \ B	0	1
0	0	1
1	1 (2)	(3)



$$D = \bar{A}B + A\bar{B} = \bar{A}B + \bar{B}A = A \oplus B$$

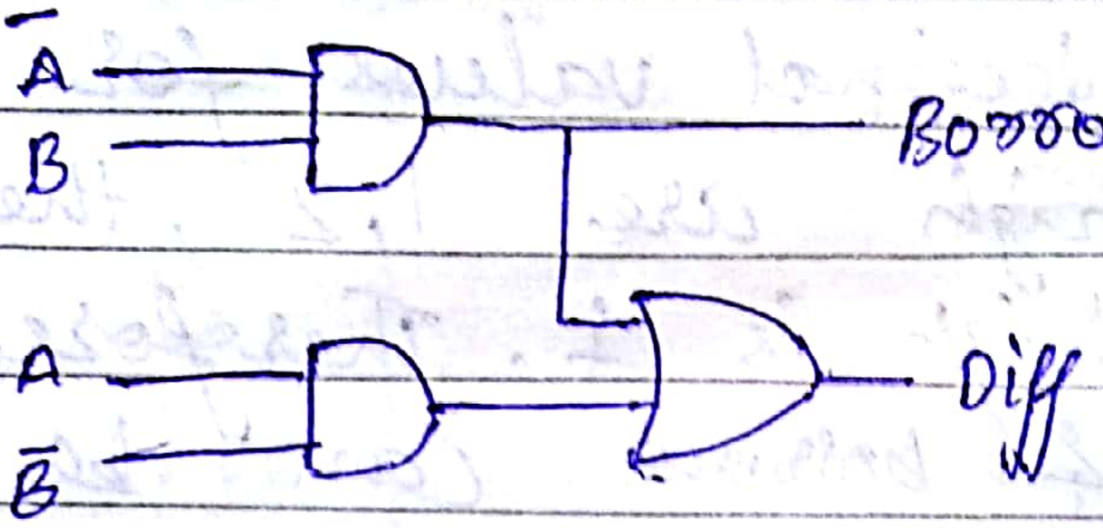
A \ B	0	1
0		1
1		

$$B = \bar{A}B$$

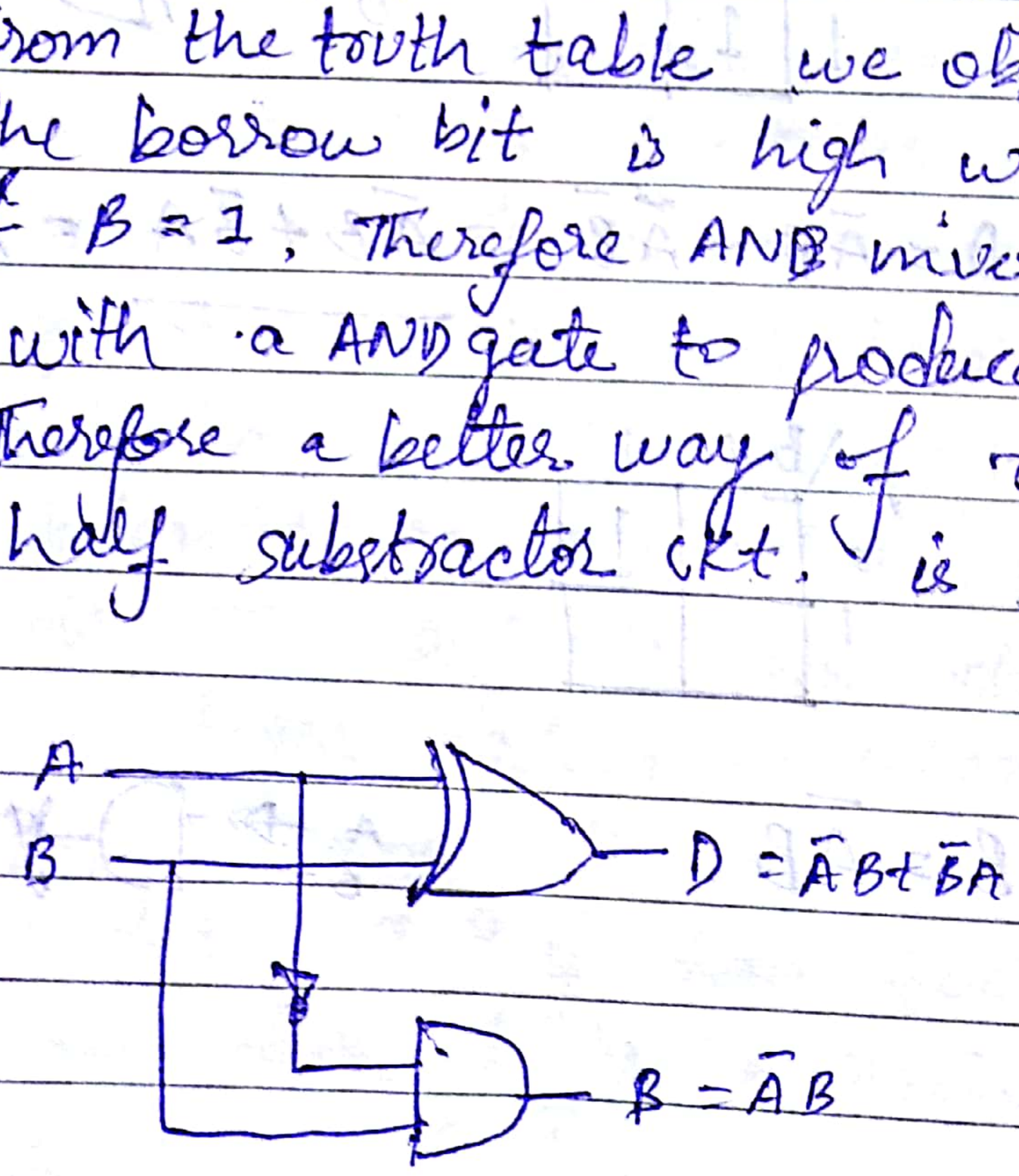


Scanned by Imran Khalid

Using the above equations the following ckt can be realised.



From the truth table we observe that the diff is high only when either of the input is '1' or high. This characteristics is similar to output of XOR gate. Therefore XOR gate can be used to produced ~~to~~ diff. bit. Also from the truth table we observed that the borrow bit is high when A is 0 & B = 1. Therefore AND inverter along with a AND gate to produce a borrow bit. Therefore a better way of realising the half substractor ckt. is shown below.

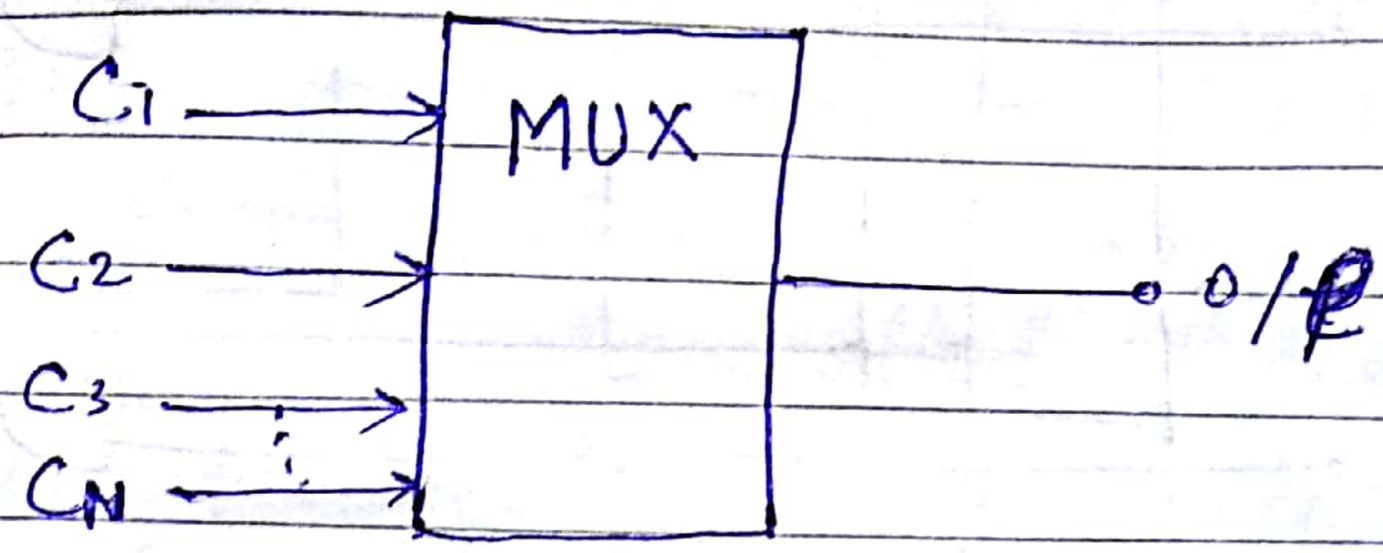


Scanned by Imran Khalid

11/08/2016

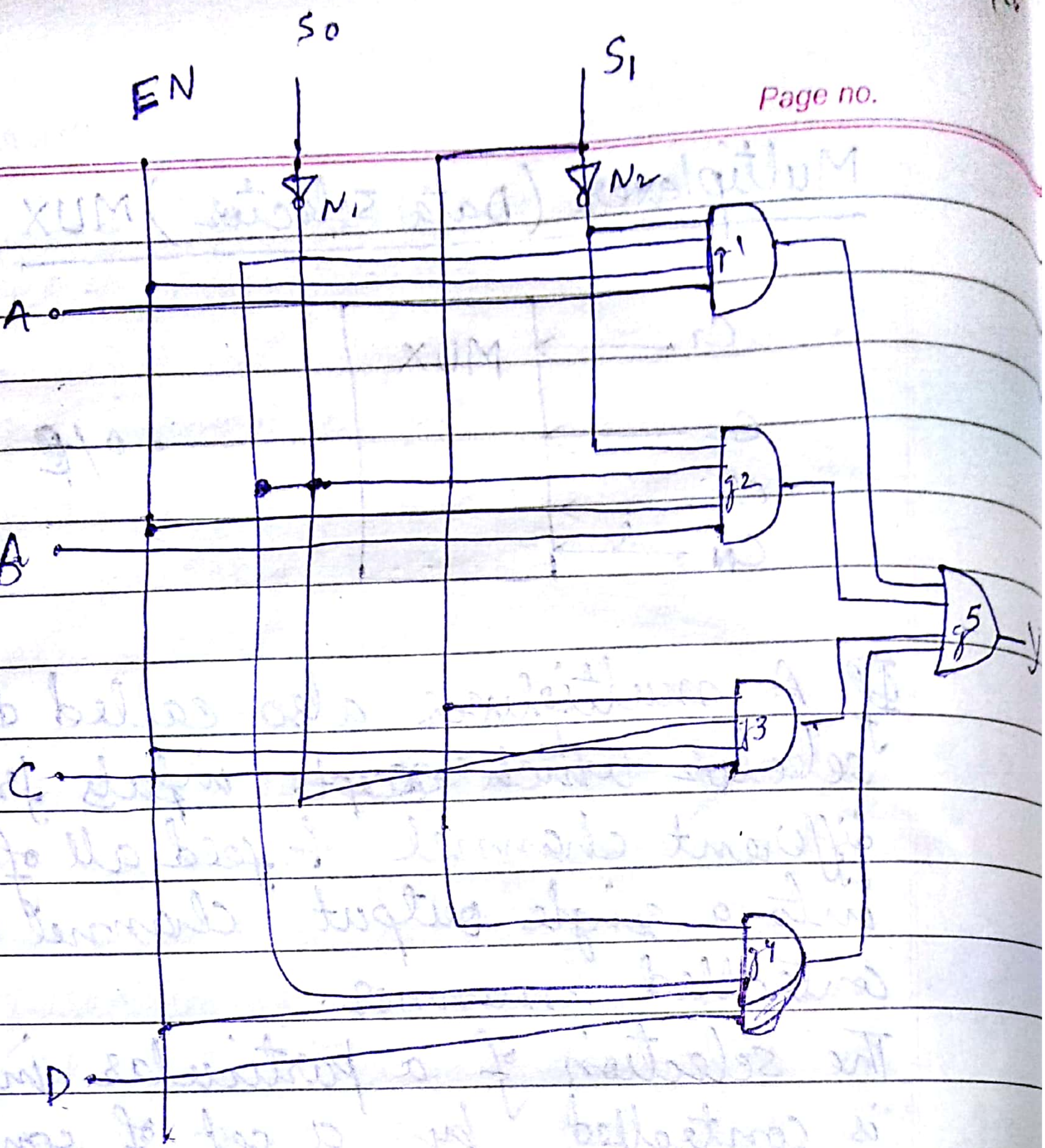
Page no.

Multiplexer (Data selector) MUX



If A multiplexer also called data selector which excepts inputs from different channel & feed all of them into a single output channel in a controlled manner.
The selection of a particular input line is controlled by a set of controlled lines. Noormally there are 2^N lines. and 'n' controlled lines whose bit combination determine which input line is to be selected.

Scanned by Imran Khalid



A, B, C, D ⇒ Input signal lines

S & S_1 ⇒ control lines

E_N ⇒ Enable line

control signal		Channel selected
S_1	S_0	
0	0	A
0	1	B
1	0	C
1	1	D

Scanned by Imran Khalid

Page no.

It consist of 4 AND gates g^1, g^2, g^3, g^4 ; one OR Gate g^5 and two not gates N_1 & N_2. A, B, C, D are the input signal lines from some memory location. As S_0 & S_1 are called controll lines to facilitates the selection of signal lines (data)

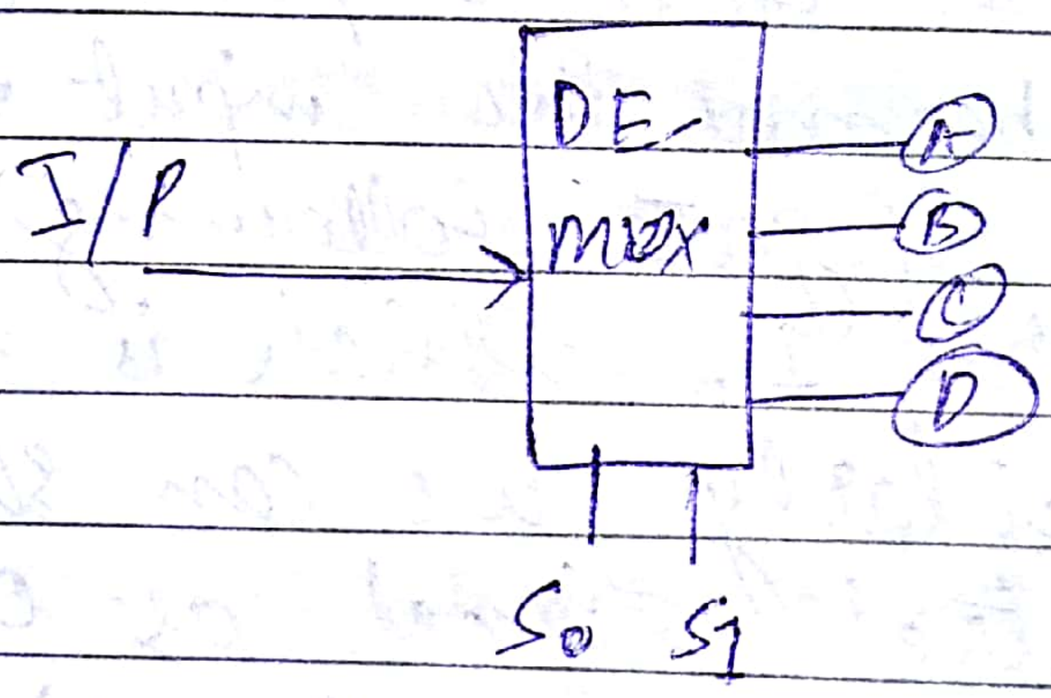
Let as $S_0 = 1$, $S_1 = 1$ then input of gate G1 will be 0011, input of gate G2 = 0111, G3 = 1011 and gate G4 = 1111. which enable (EN) to 1. The gate G4 gets enable while the Others gate G1, G2, G3 gets disabled. The all the AND gates following their laws will output 0001 which become the input of OR gate g^5. The OR gate following its laws will output 1, which is channel D. similarly we can show with control signal as 00, 01, 10 The MUX will output the signal line A B & C.

Scanned by Imran Khalid

De-Multiplexer (DE-MUX)

A DE-MUX also called decoder is a ckt. which accepts information on a single input line or channel and feeds them to multple output channel in a control manner. It is opposite to multiplexer.

The selection of the particular output line is controlled by a set of controlled signal line normally there are 2^n output lines and 'n' controlled lines whose bit combination determines which output line is selected.



Scanned by Imran Khalid

17/08/2016

Page no.

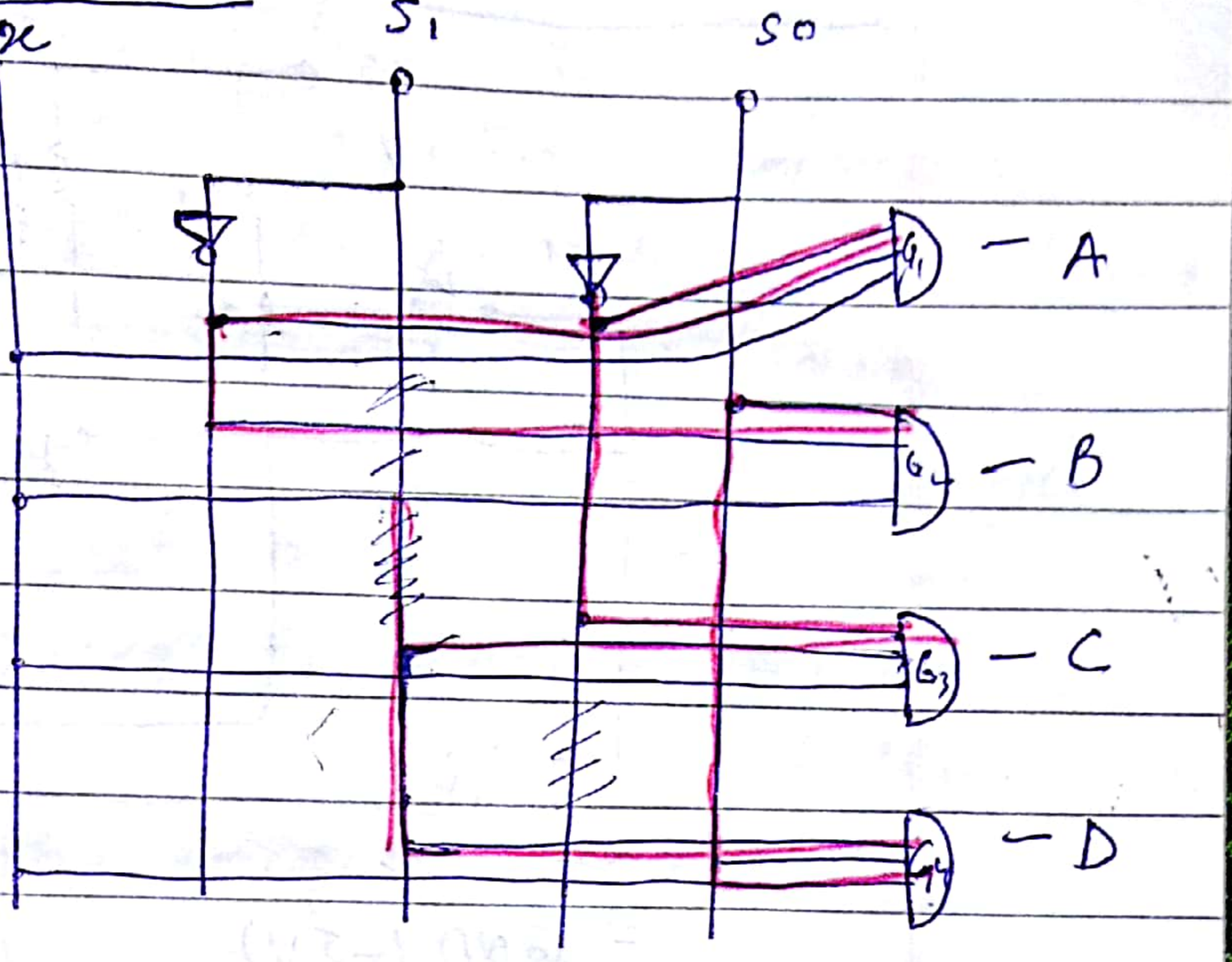
1 x 4 DE-MUX

3.

x = Output signal lines

$S_1 S_0$ = control lines

A, B, C, D = op channel

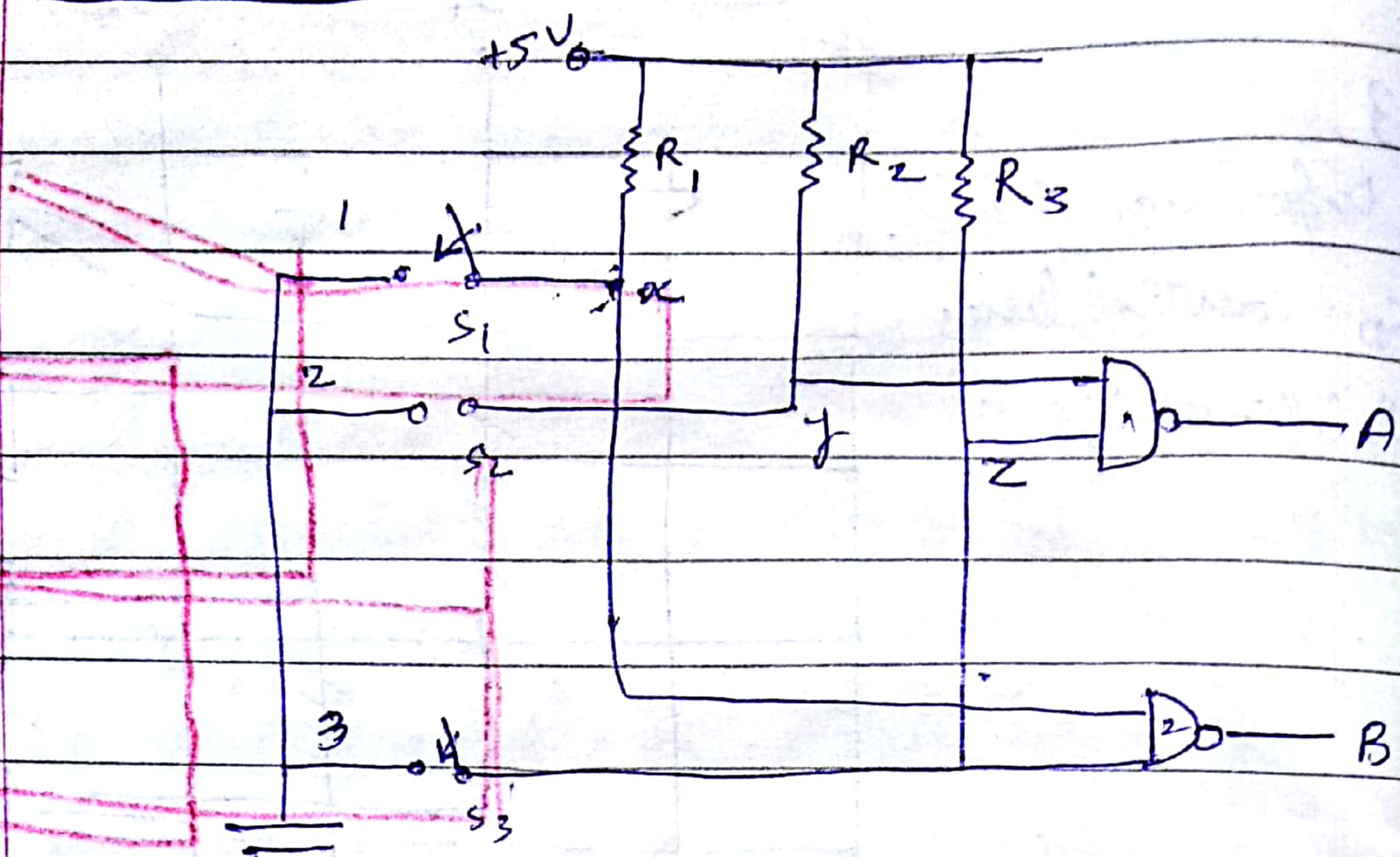


Control signal		O/P channel
S_1	S_0	
0	0	A
0	1	B
1	0	C
1	1	D

It consist --

Scanned by Imran Khalid

Encoders



$R_1 = R_2 = R_3 = R$

Dec	Binary o/p	
	A	B
0	0	0
1	0	1
2	1	0
3	1	1

encoders are computational logic ckt. which accept one or more input data and generate a multibit binary output. They are used for translating decimal keyboard, as in calculators, computer, into BCD output code.

The above ckt consist of two NAND gates which provide two bit

DELTA My NoteBook

Scanned by Imran Khalid

t_3 = logic 1

Page no.

binary code as output. Initially all the switches remain open. let the switches be provided decimal no. 1, 2, 3. let the switch S1 be closed & switches S_2 & S_3 are get open then current will flow through register 1 such that a current will flow IR drop (voltage drop) = 5 V whereas NO current will flow through the registers R_2 & 3. Therefore J, 3 will be at five volts. Therefore input of NAND gat 1 will be one one (1N) and the input will be 0 & 1. The NAND gate following theier laws will outpu is zero one (01) which is binary equivalent of decimal 1. similarly.

Scanned by Imran Khalid

18/08/2018

Page no.

Parity Bit Generator

when digital signals are transmitted from one point to another a noise impulse may change the logic level of a data bit!
To declect errors induced in the data due to noise or some other reasons we add and an extra bit to the transmitted signal it is known as parity Bit. It can 0 or 1.
If the parity bit is added such as to make an even no. of 1's in the binary data it is known as even parity. If the parity bit are so added to given odd no of 1's in the binary data : It is known as odd pailty.

Ex 1:- ODD Parity

Parity	Data	Total no. of 1s
0	1010110	4
1	1010110	5
0	1010111	5
1	0010010	3
1	0000000	1

Scanned by Imran Khalid

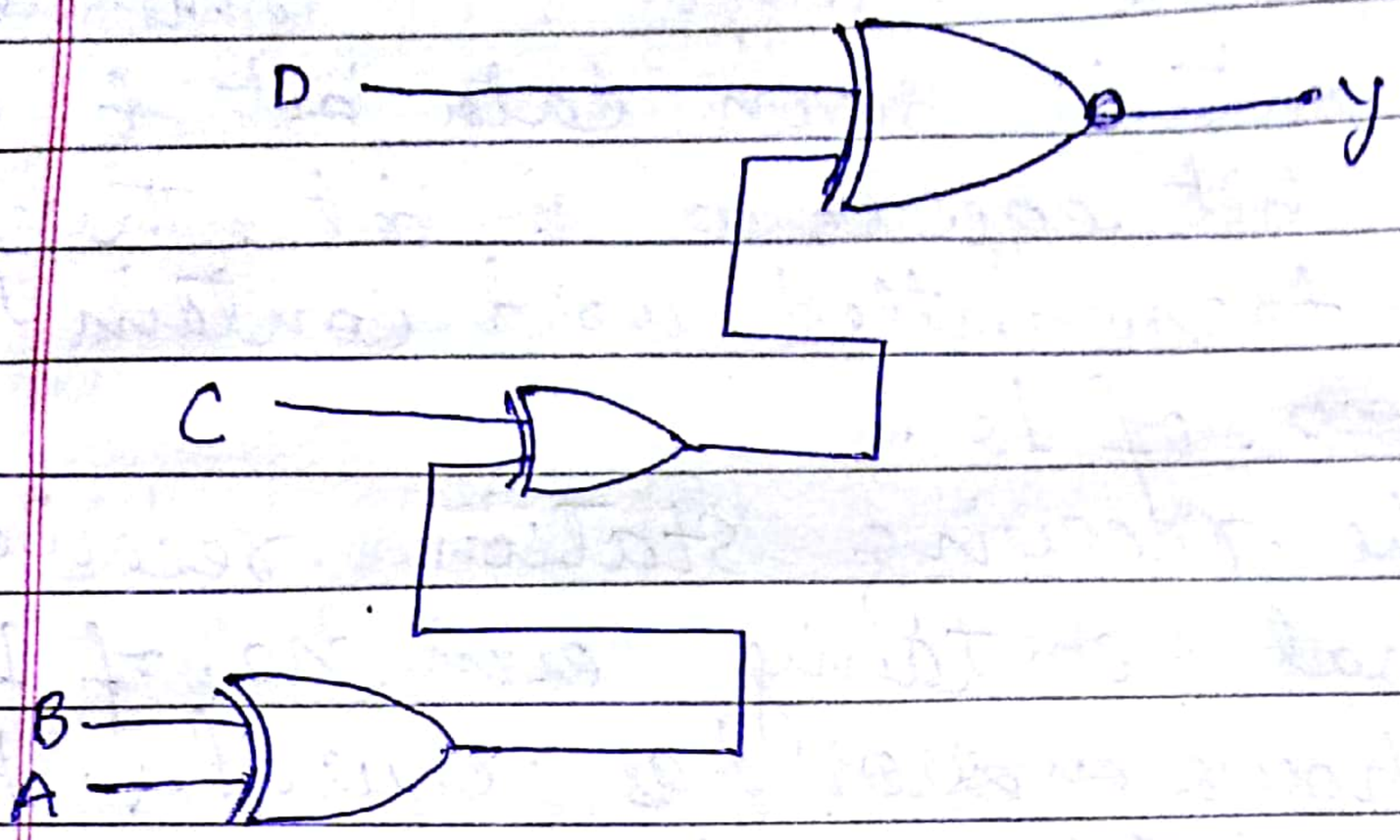
In the above example, the transmitted word contain seven data bit & one parity bit equals to 8 bit. Therefore each transmitted word contain an odd no. of 1's.
If the receiving station receive the signal containg even no. of 1's, It shows an error has occured & the transmitting station is required to re transmitt the complete data.

Ex :- EVEN parity

Parity	Data	Total no. of 1's
1	1010111	6
1	0000111	4
0	0010010	2

However, If the transmitted data contains two or more errors that is 2 or more bit change than the error remains undetected. and others methods are implayed or used suchas check sum, Parity Data codes, etc

Scanned by Imran Khalid



The ckt. consist of three XOR gates through which BCD data is given at the input. If the data input has odd no. of 1's. Then $y = 1$. If the data input contain even no. of 1's then $y = 0$. The output y may be added to the data as the parity bit. This makes and even parity generator. To get odd parity and inverter is included to the output line to the logic ckt.

BCD Code				Even parity	Odd parity
D	C	B	A		
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0

DELTA My NoteBook

Scanned by Imran Khalid

22/08/2016

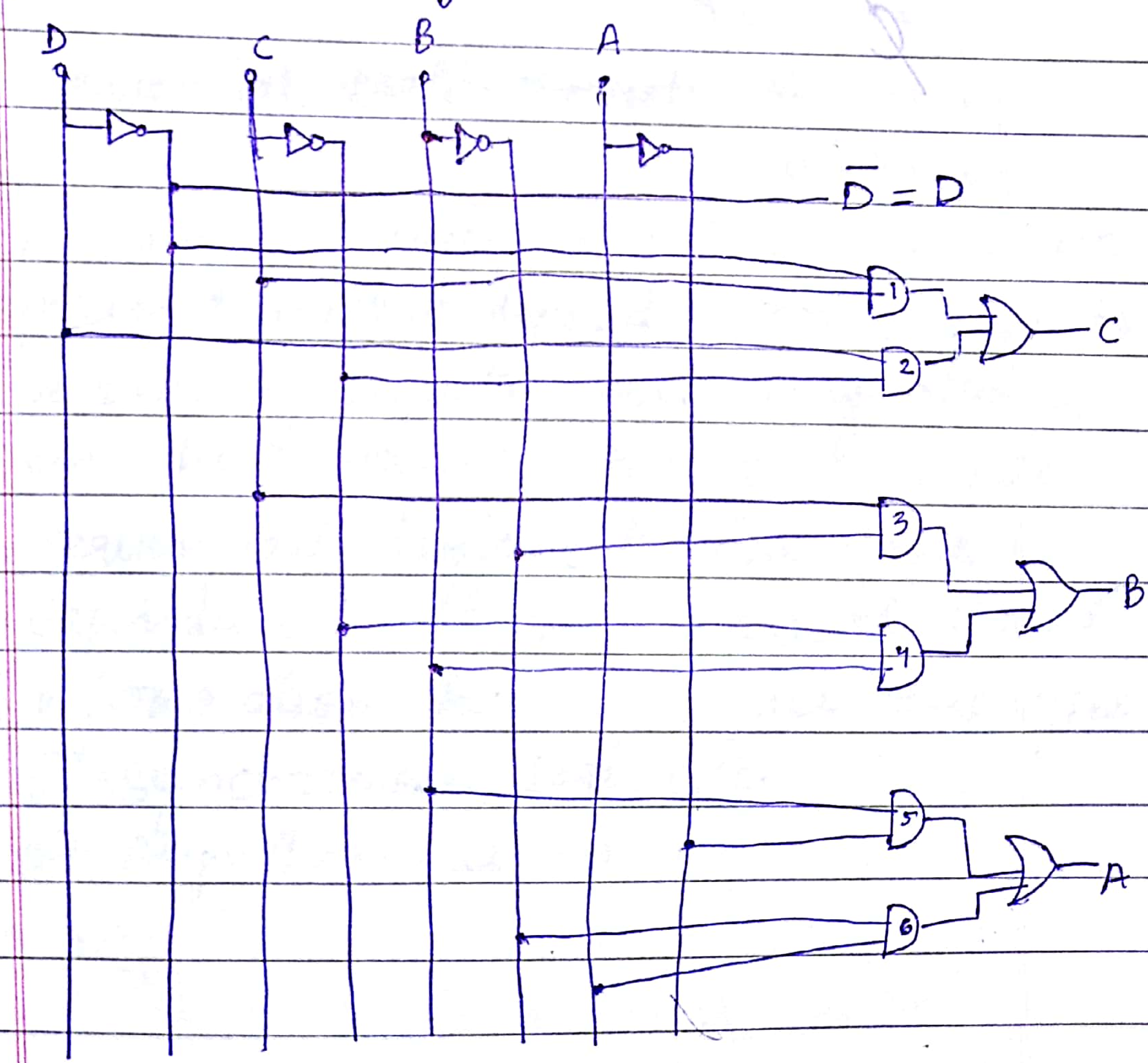
Page no.

0101	0	1
0110	0	1
0111	1	0
1000	1	0
1001	0	1

Binary to Gray Code converter

1001 ← Binary
1101 ← Gray

1001
D C B A



This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

Page no.

→ Convert $(1001)_2$ to Gray code.

Sol. The above logic ckt

$A = 1$

$B = 0$

$C = 0$

$D = 1$

Then $\overline{A} = 0$

$\overline{B} = 1$

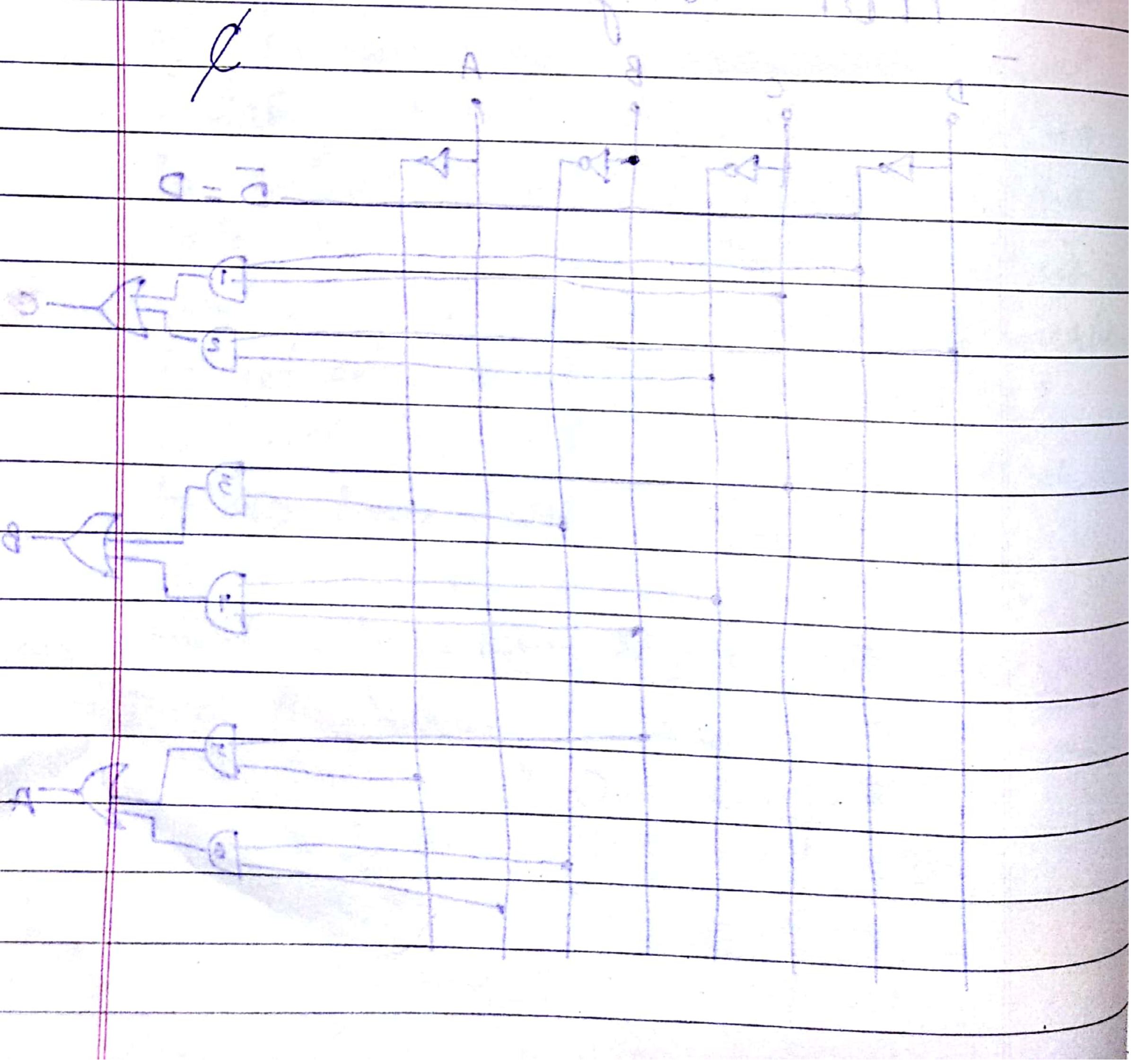
$\overline{C} = 1$

$\overline{D} = 0$

$(1101)_{Gray}$

1001

A B C D.



Scanned by Imran Khalid

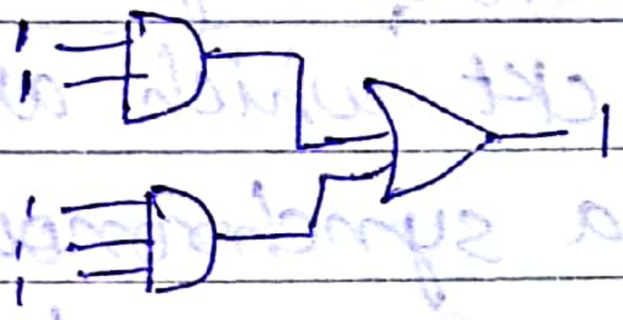
Unit - III

Page no.

Combinational logic circuit.

A combinational logic circuit is one in which the state of the output at any instant is entirely determine by the state of the input at that time. It is a memory less logic network.

$$y = x\bar{x}_2 + x_1x_2x_3$$



sequencial logic circuit

A sequencial logic circuit is one whose present output depend upon previous sequence of inputs and may also be on the current state of inputs. sequenciall dogic ckt are time dependent and remember of stored information. As SLC's are two types

① Synchronous logic ckt.
② Asynchronous " ".

Page no.

① synchronous logic ckt.

Sequencial ckt's which are clocked are called synchronous ckt. They have a master oscillator which provide regular timing pulses. & events are allowed to occur during one of these timing pulses. They are totally depend upon clock.

② Asynchronous logic ckt.

Sequencial ckt which are not clocked are called a synchronous ckt. In these ckt. events occurs when the previous event is completed. There is no need to wait for a timing pulse.

Flip flop (Latch or Bestable multivibrator)

A flip-flop is a sequencial logic device that perform the function of storing and switching b/w states (0, 1). since a flip flop has two possible states that is called bistable device. It can remain in a particular state indefinetly, as long as power is delevered to the ckt, or and external signal is applied to its inputs to change its state.

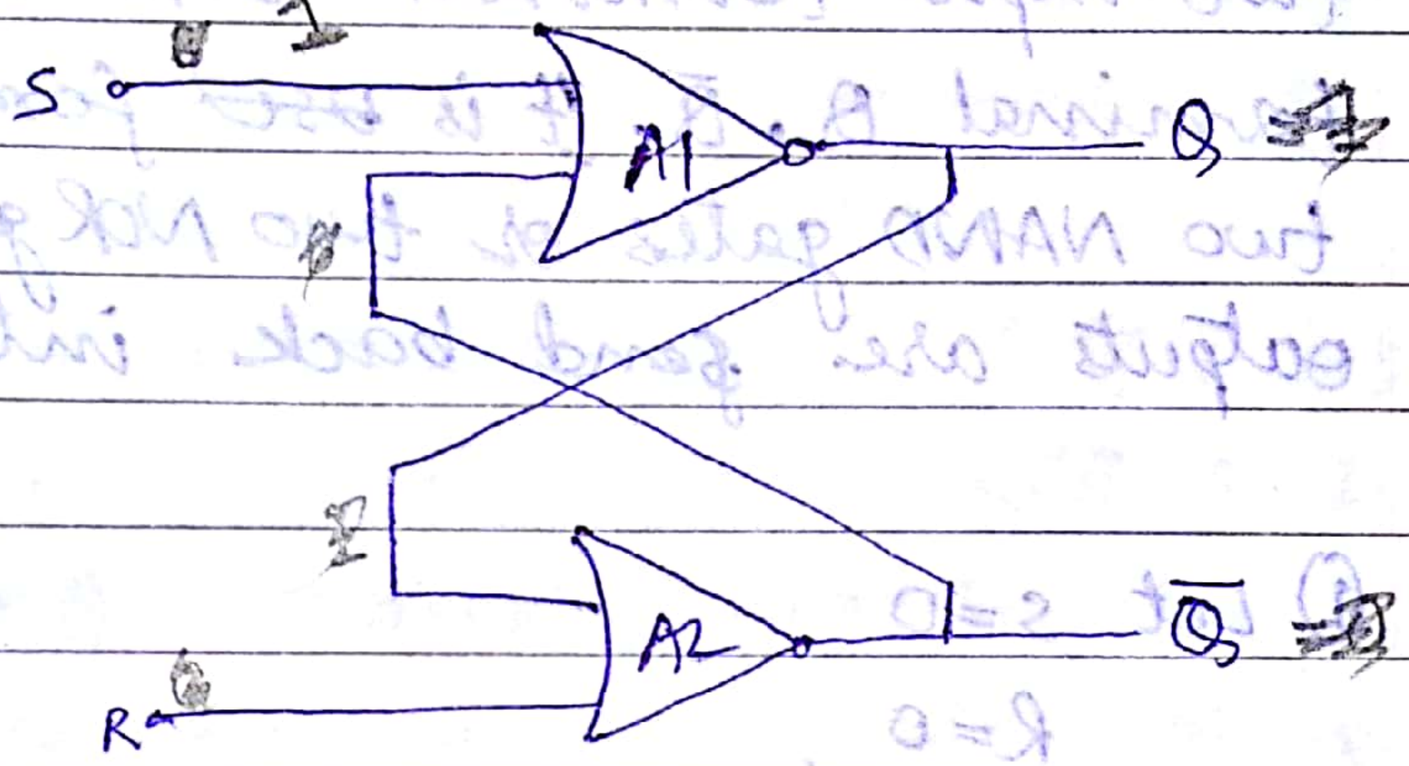
DELTA My NoteBook

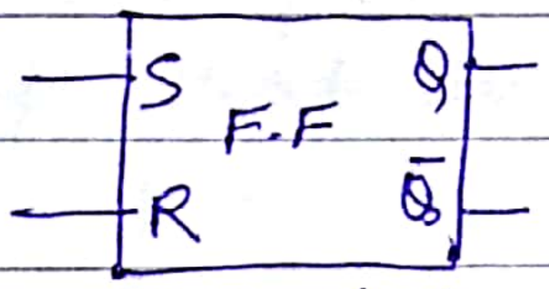
Scanned by Imran Khalid

Page no.

Classification of flip-flop

1. S.R. Flip flop (S.R. Latch)
2. T- Type Flip flop
3. J.K flip flop
4. Master slave flip flop
5. D-Type flip flop





Block Diagram

T.T

S	R	Q	$\bar{Q}$	comment
0	0	Q	$\bar{Q}$	No change
1	0	1	0	set
0	1	0	1	Reset
1	1	—	—	forbidden

Scanned by Imran Khalid

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

It is a set flipflop also called S R. Latch. It has two input terminal S, R & two output terminal Q, $\bar{Q}$. It is ~~use~~ formed by using two NAND gates or two NOR gates. whose outputs are send back into the input.

① Let S = 0

R = 0,

Q = 0

$\bar{Q}$ = 1

When the input of Gate A1 become 0 1 and the input gate A2 : 0, 0. The gate A1 get disabled and therefore its output Q remain Q = 0. The gate A2 gets enabled and ~~its~~ therefore its output $\bar{Q}$ = 1. From the above result it is observe that applying input conditions as S = 0, R = 0 do not change in output condition. Hence this condition is never allowed in SR.

Scanned by Imran Khalid

flip-flop

(2) let S=1, R=0, and
Q=1

Q is defined as when S=1 then Q=1.
when the set input is given S=1
then the gate A2 following its laws
gets disabled

$A_2 = 0$ or $\overline{Q} = 0$.

since $\overline{Q}$ is complement of Q, Q should be equal to one. Hence with S=1 and R=0, $\overline{Q}$=1 and Q=0. The flip flop will remain in this state till a reset is pulse is applied we can also say that the flip flop has stored one bit in its memory. The R=1 input can only be applied after the both the input are in 0 0.

(3) S=0
R=1
$\overline{Q}$=1

when the set input mode S=0, R=1 then the gate A1 gets disabled and NOR gate following its law with output zero (0).

($A_1 = 0$ or $Q = 0$),

DELTA My NoteBook

Scanned by Imran Khalid

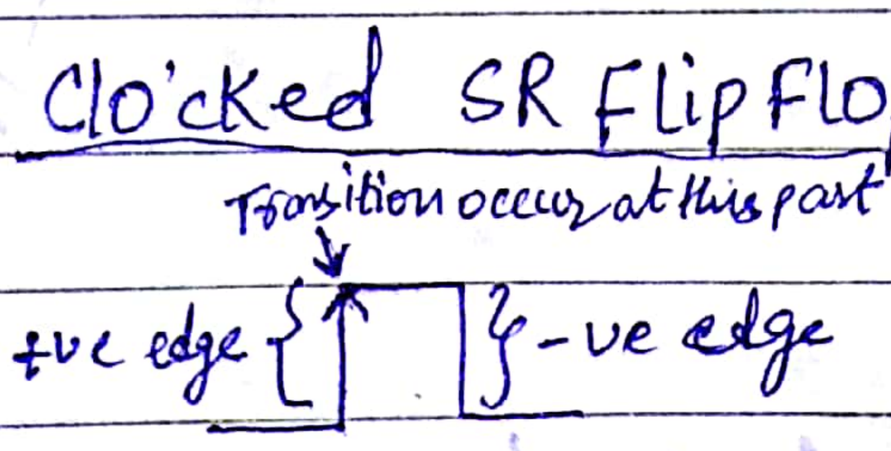
since $\bar{Q}$ is a compliment of Q, should Q be 1.

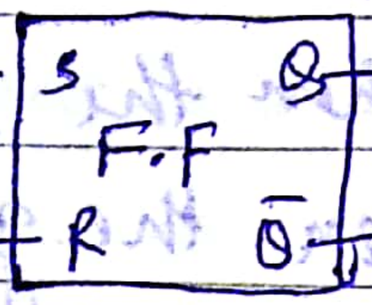
Hence with S=0, R=1, Q=0 and $\bar{Q}$=1. that is flipflop is put back into its orginal condition. The flip flop will remain in this state with another set input pulse is applied. we can also say the flip flop has stored another one bit that is zero bit in its memory.

(4) S=1 & R=1

are made equal to 1 forces the output of both the gates equal to 0. Q=$\bar{Q}$=0, At the same time. This result violets the basic defination of a flipflop which requires Q to be compliment of $\bar{Q}$. Hence it is not used and known as forbidden state.

Clocked SR FlipFlop





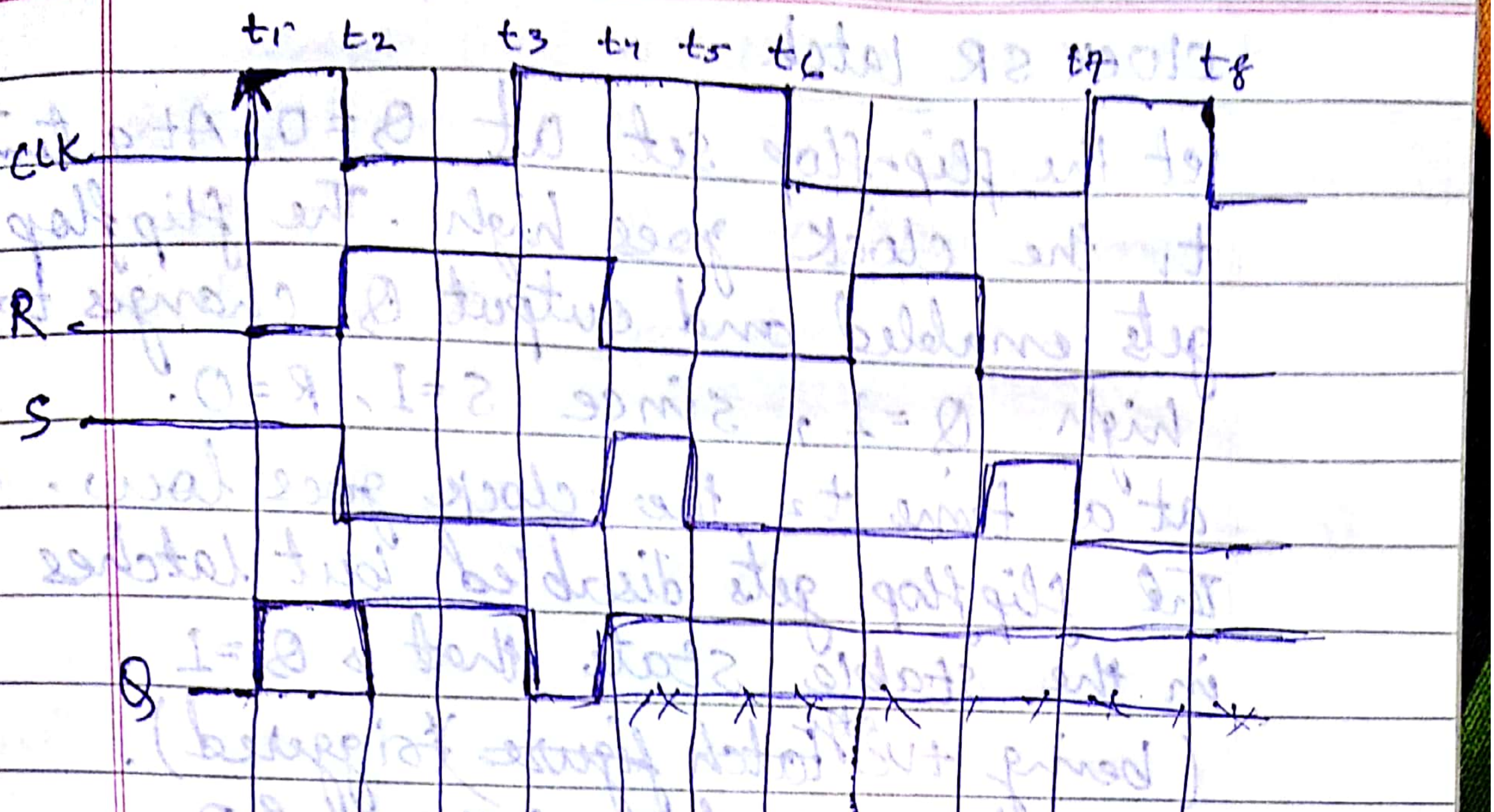
+ve edge triggered flip flop.

Scanned by Imran Khalid

24/08/2016

Timing Diagram

Page no.



A clocked signal is a periodic square wave or a periodic collection of pulses. which cause the flip flop to change its state at a specific part of their shift shape. The specific portion of the shape or signal is called edges.

R	S	Q	$\bar{Q}$	Command
0	0	0	0	no changed
0	1	0	1	
1	0	1	0	
1	1	?	?	

Scanned by Imran Khalid

20/08/2016

Page no.

Clock SR latch

let the flip-flop set at $Q=0$. At a time t_1 the clock goes high. The flip flop gets enabled and output Q changes to high $Q=1$, since $S=1$, $R=0$.
at a time t_2 the clock goes low. The flip flop gets disabled but latches in the stable state that is $Q=1$ (being +ve edge triggered).
let between t_2 & t_2, both S & R change their state that is $S=0$, $R=1$. since the clock is low the flip flop remain disabled and hence in the output Q remain high.
At t_3 the clock goes high the flip-flop gets enabled and will repond to any changes in S & R. Since S goes low & and goes high, the output Q changes to low.
At t_4 the flip-flop is still remain enabled and will respond to the changes in the input. since at t_4 R goes low and S goes high, the output Q again goes high.

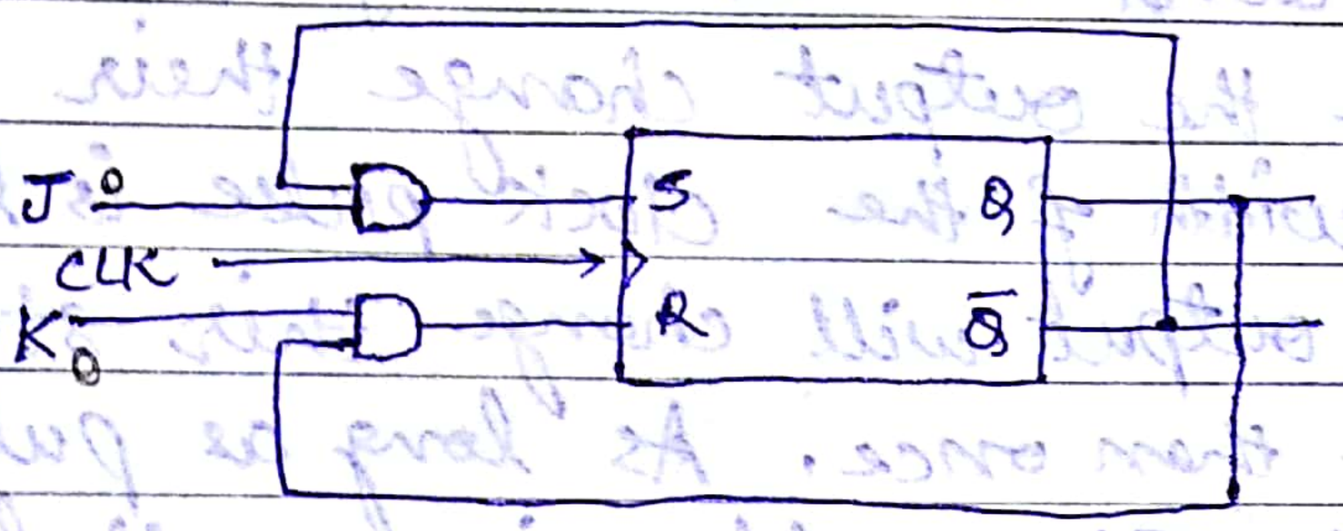
Between t_4 & t_6 the clock remain high. The flip flop remain enabled are remain low and S goes low. The output will remain high because at $R=0$, $S=0$

DELTA My NoteBook

Scanned by Imran Khalid

No change will occur in the output. Between t_6 & t_8 No further change will occur in the output since both S & R remain low.

J.K flip flop



J	K	Q-Response
0	0	unchange
0	1	Q = 0 (Reset)
1	0	Q = 1 (set)
1	1	Flip

let J = K = 0

let Q = 1

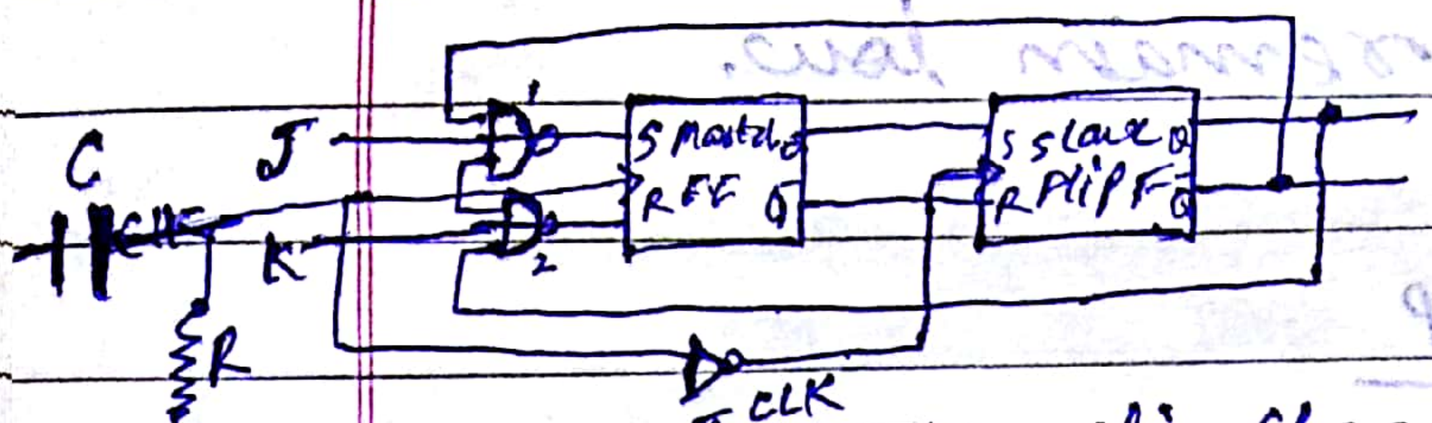
DELTA My NoteBook

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

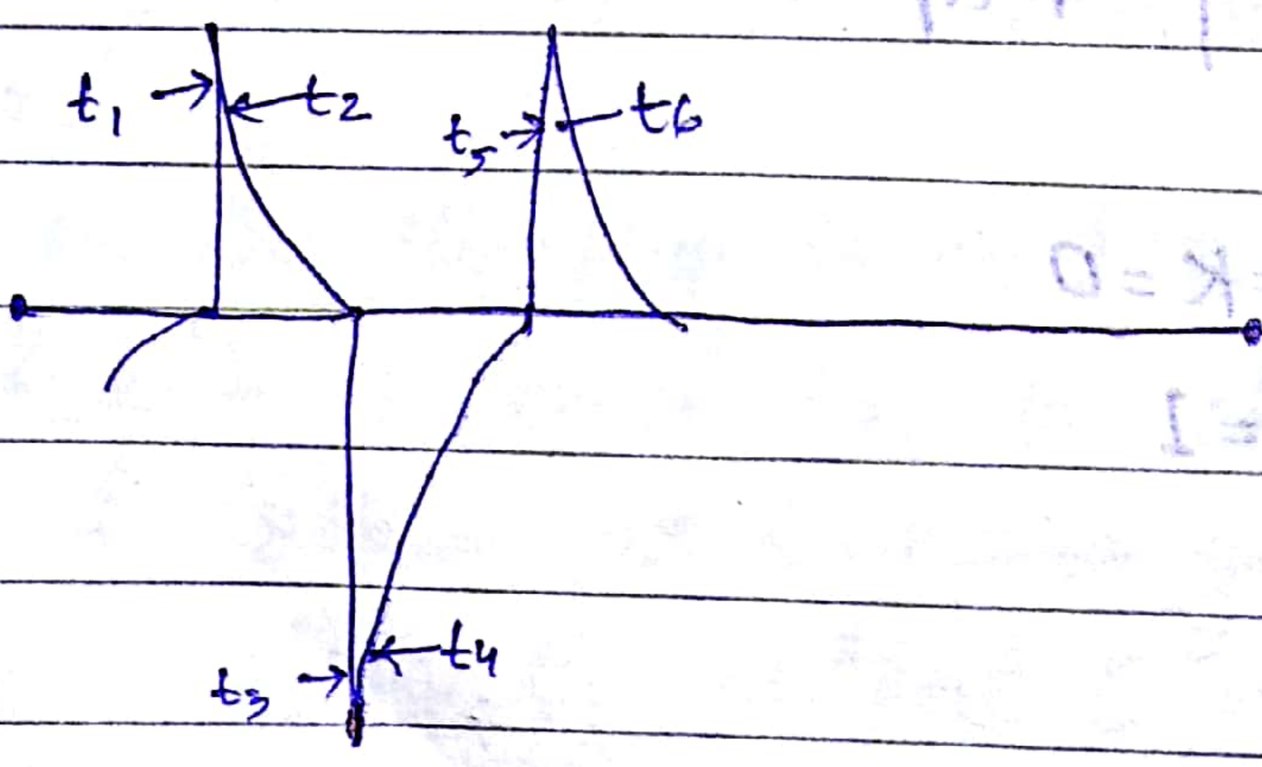
Master Slave JK flip flop

Race around problem



clk pulse
trigger
Integreater

Note:- In JK flipflop with J=1, K=1 and with the arrival of +ve clock pulse the output change their state. If width of the clock pulse is large then output will change their state more than once. As long as pulse exist. This problem is called Race around problem and is retified by using master slave flip flop as shown in the figure.



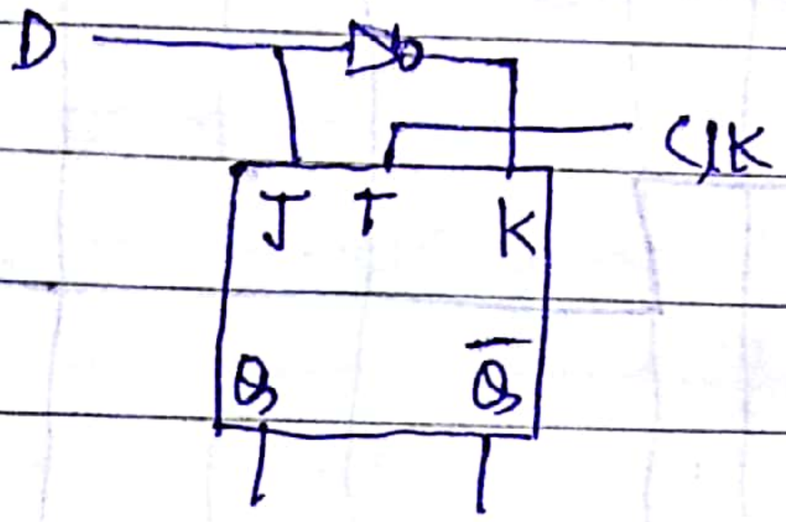
Scanned by Imran Khalid

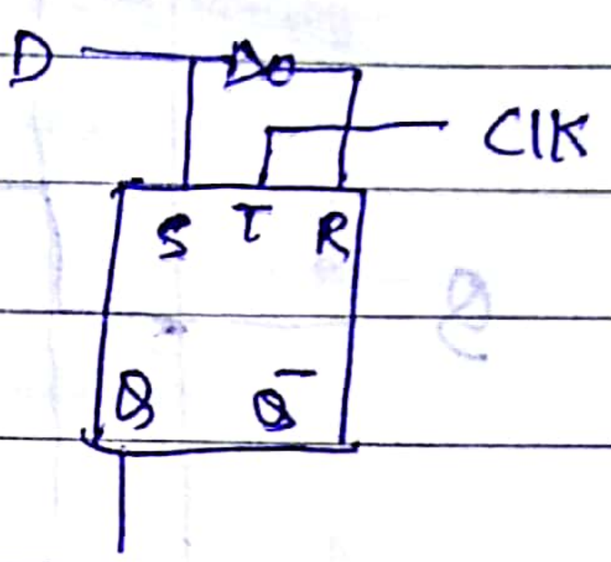
Unit - IV D = S 21/08/2016

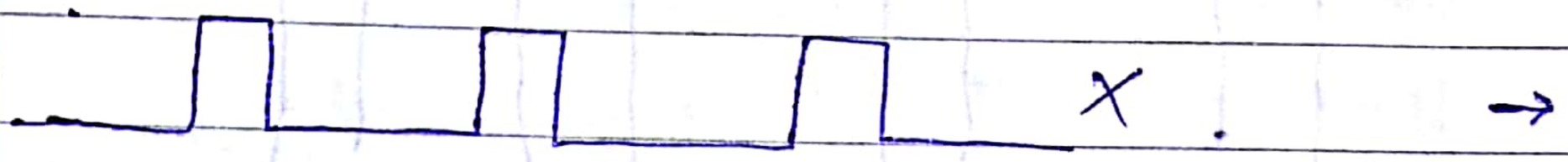
Registers

CLK	D	Q_n
0	X	Q_n
1	0	0
↑	1	1

D - Flip flop





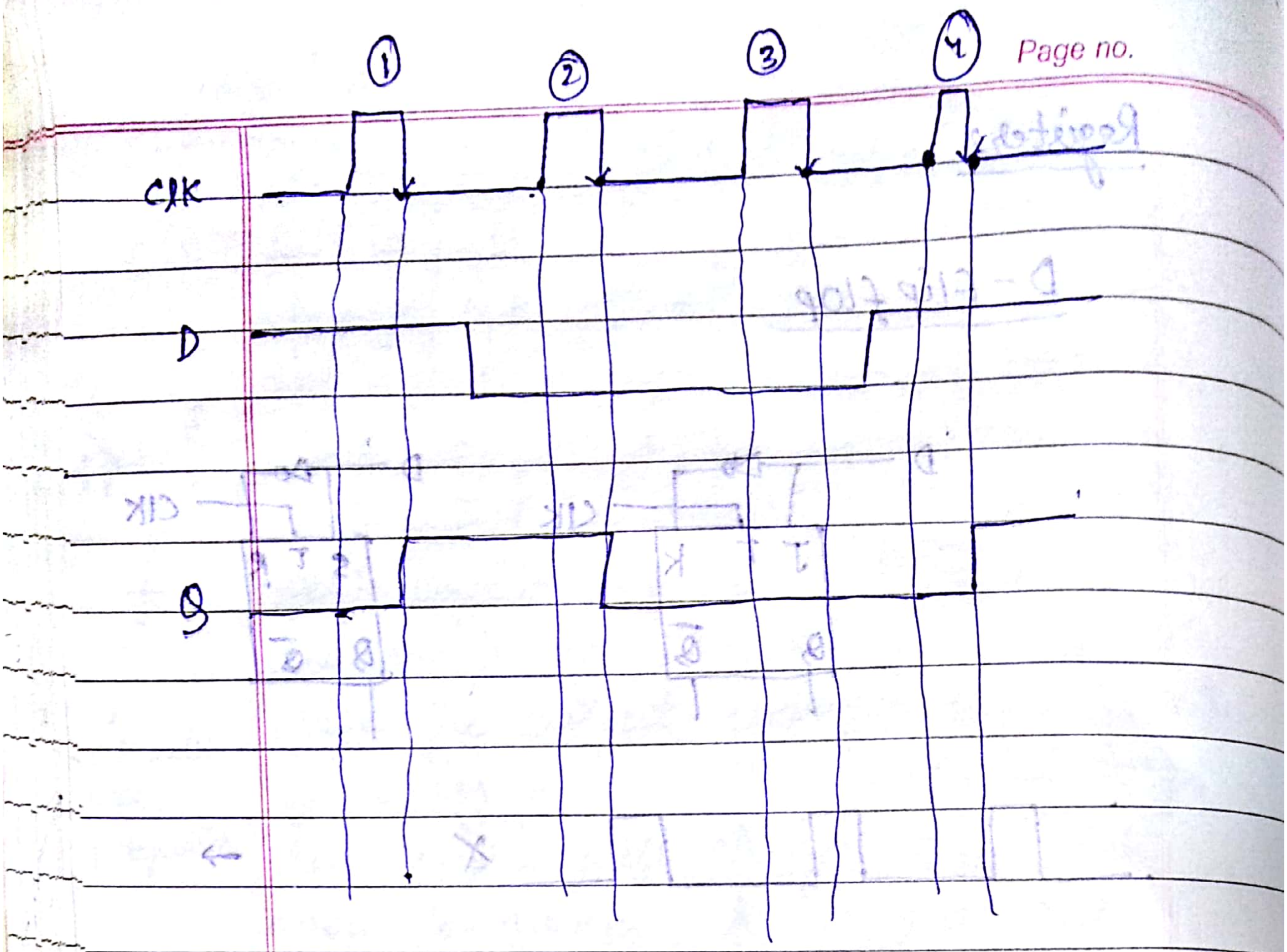


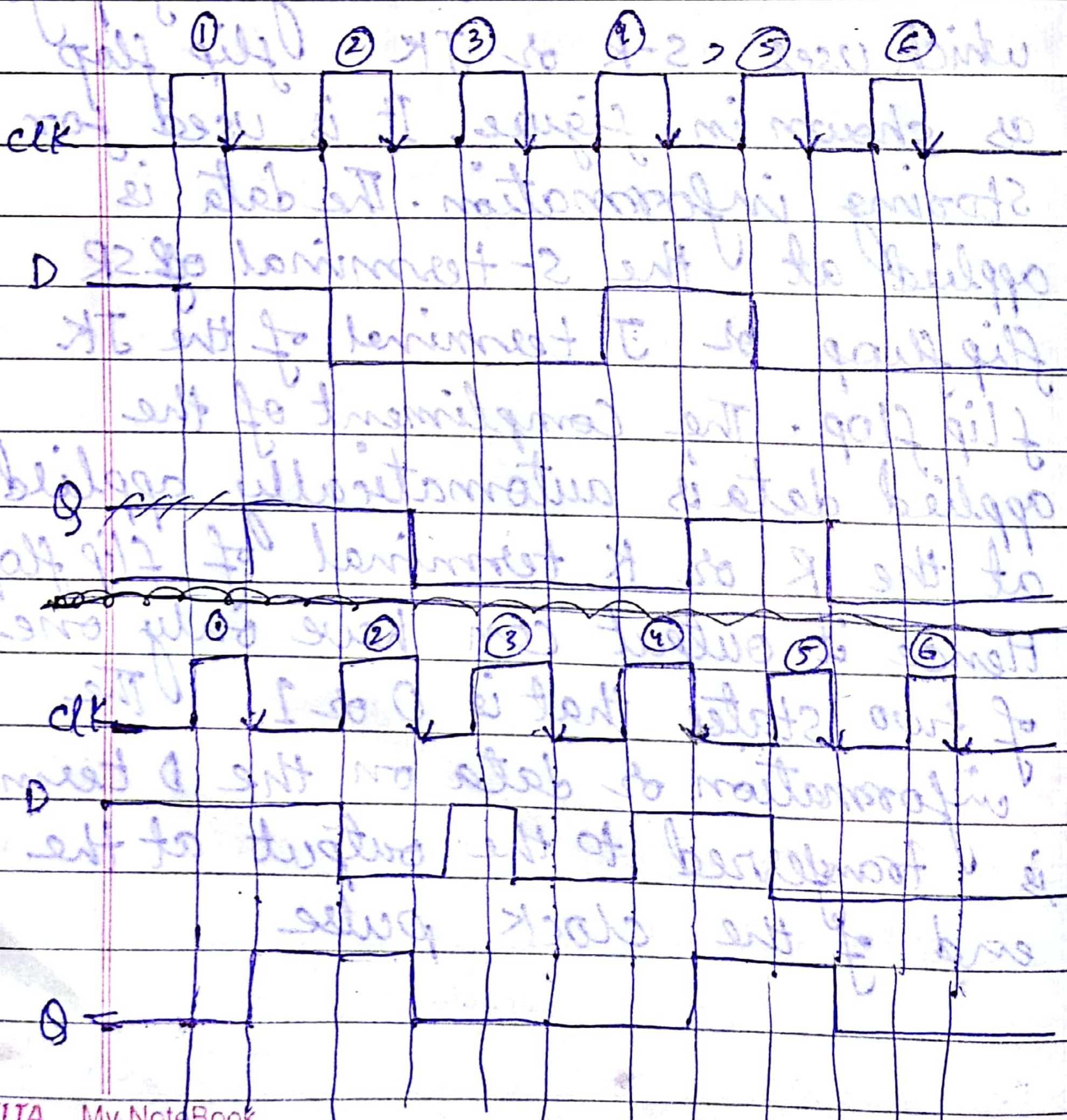
It is also called data or delayed flip-flop which uses S-R or JK flip flop as shown in figure. It is used for storing information. The data is applied at the S-terminal of SR flip flop or J terminal of the JK flip flop. The compliment of the applied data is automatically applied at the R or K terminal of flip flop. Hence it output can have only one of two states that is 0 or 1. The information or data on the D terminal is transferred to the output at the end of the clock pulse.

DELTA My NoteBook

Scanned by Imran Khalid

Page no.





DELTA My NoteBook

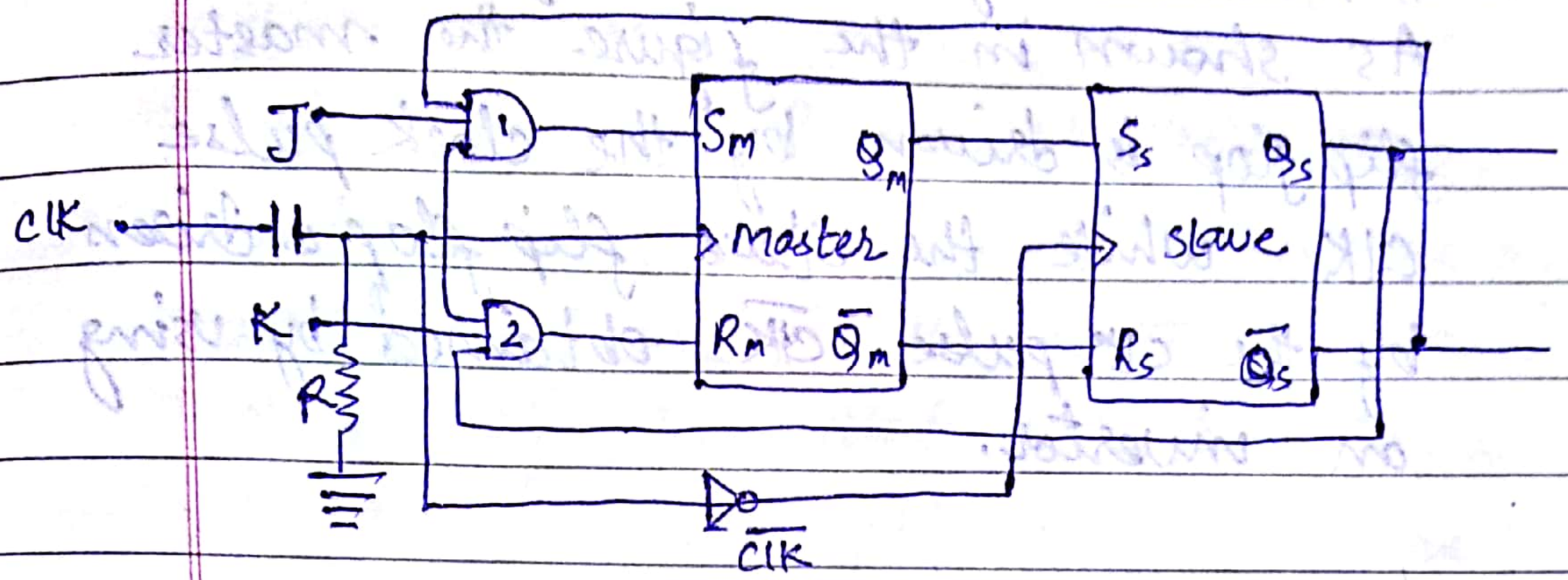
Scanned by Imran Khalid

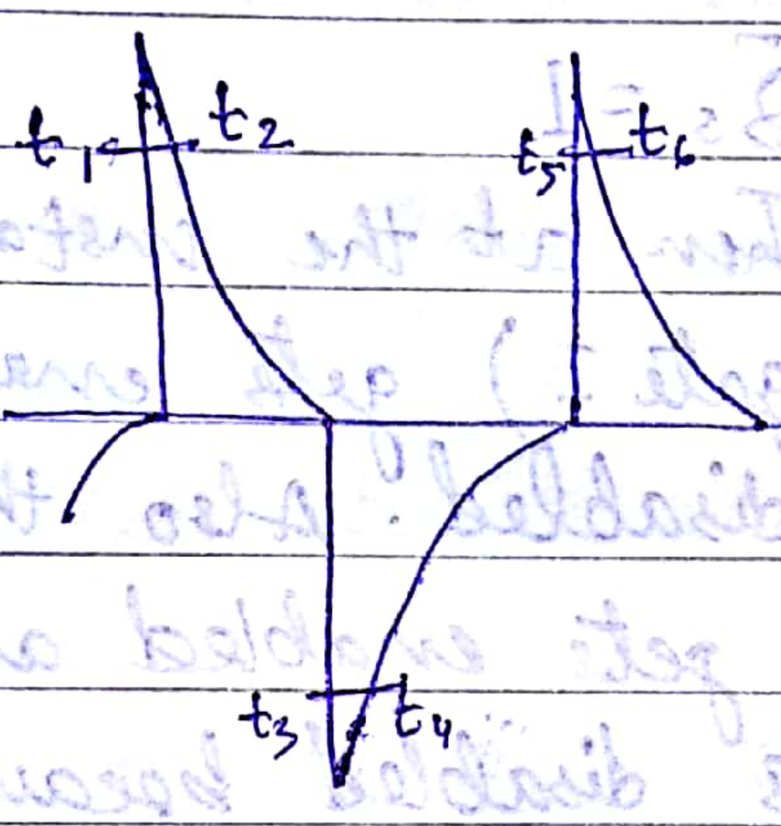
01/09/2016

b)

Page no.

Master Slave J.K FF





Problem of race around (changing of the output more than once during one clock pulse) can be avoided completely by using a master slave ckt as shown in the figure.

It consist of two SR flipflop which are connected in JK mode of operation. The first flip flop act as master whereas the second flipflop act as slave flip flop. The output of the master flip flop act as the input to the slave flip flop.

Scanned by Imran Khalid

The output Q_s of the slave flip flop is fed back to the input of the master flip flop through AND gates 1 & 2. As shown in the figure the master flip flop is driven by the clock pulse CLK while the slave flip flop is driven by the clk pulse $\overline{CLK}$ obtained by using an inverter.

Operation :-

$J=1$, $K=1$, $\overline{Q}_s=1$.

Also let $CLK=1$. Then at the instant T_1 the Gate 1 (AND gate 1) gets enabled and the Gate 2 disabled. Also the master flip flop gets enabled and the slave flip flop gets disabled because $CLK=0$. The data ~~at~~ input at point J & K are transferred to the master flip flop that i.e., $Q_m=1$, $\overline{Q}_m=0$. The slave flip flop being disabled, its output Q_s & $\overline{Q}_s$ which are fed back to the master flip flop, remain the same. At T_2 Gate 1 & 2 get disabled and remain inactive till the instant T_3. Therefore when Q_s & $\overline{Q}_s$ not change the input of master flip flop also do not change and hence the output Q_m & $\overline{Q}_m$ remain stable

DELTA My NoteBook

Scanned by Imran Khalid

01/09/2021

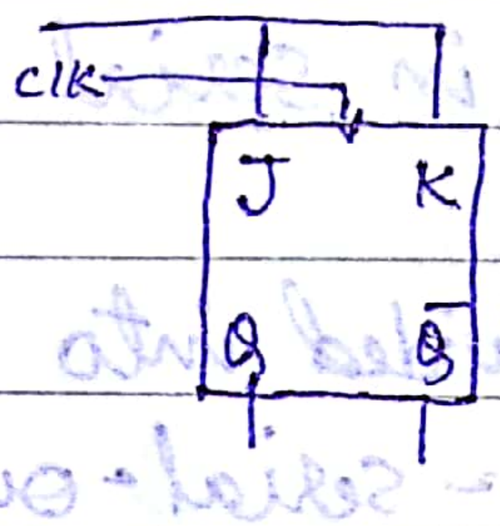
Page no.

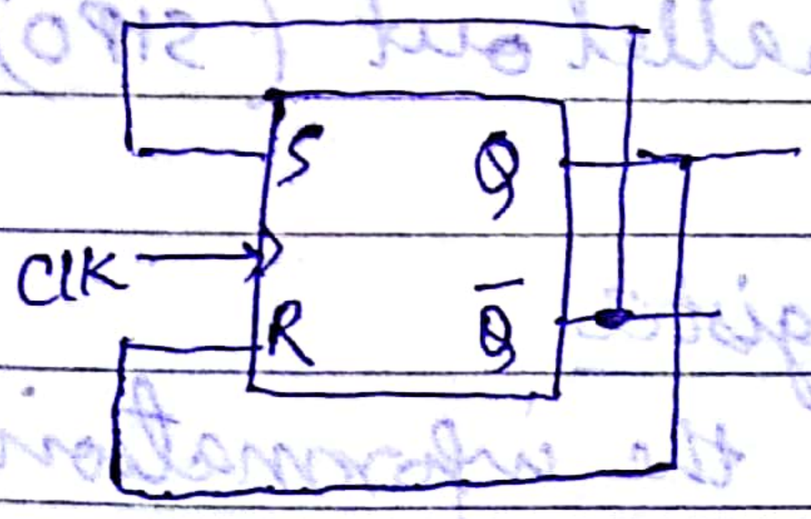
that is 1 & 0. Thus the race around problem is controlled.

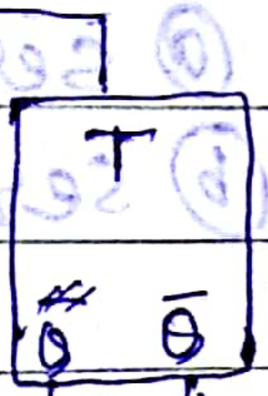
let the clk pulse clk = 0. AT T_3 the slave flip flop gets enabled and the data output of master flip flop, which are input to the slave flip flop are transferred to the output of the slave flip flop that is $Q_s = 1$, $\bar{Q}_s = 0$. At T_4 the slave flip flop also get disabled and remain inactive till T_6.

since till the output of the slave flip flop follow the ouput of master flip flop it gets its master flip flop.

Type T. flip flop







symbol

Scanned by Imran Khalid

05/09/2016

Registers

Page no.

The register is a group of flip-flops in which each flip-flop is capable of storing one bit of infoormation. In digital systems we foequently need toansfer of data from one flip flop to another flip flop. Therefore on Array of flipflops that perform the function of shifting the data is called a shift register. Usually D-Type lathes are used in cascade to constructor shift register. RS and JK flip-flops can also be used as register. Register are categories as no:-

1) serial shift Register
In these register information is shifted to another register one bit a time in serial fashion or manner.
It is sub divided into ..
ⓐ serial-in - serial-out (SISO)
ⓑ serial in paralled out (SIPO)

2) Parallel shift Register
In these registers the information is shifted to another register at the same time in paralled fashion.

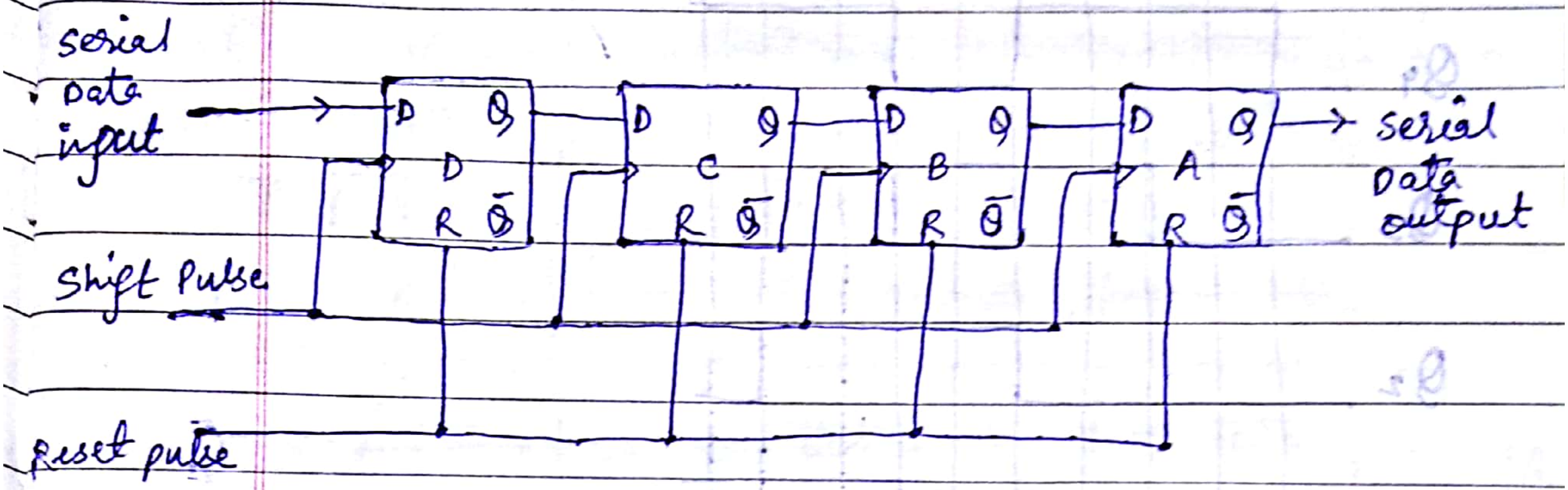
Scanned by Imran Khalid

Page no.

It is sub-divided into :-

(a) Parallel in parallel out (PIPO)

(b) Parallel in serial out (PISO)

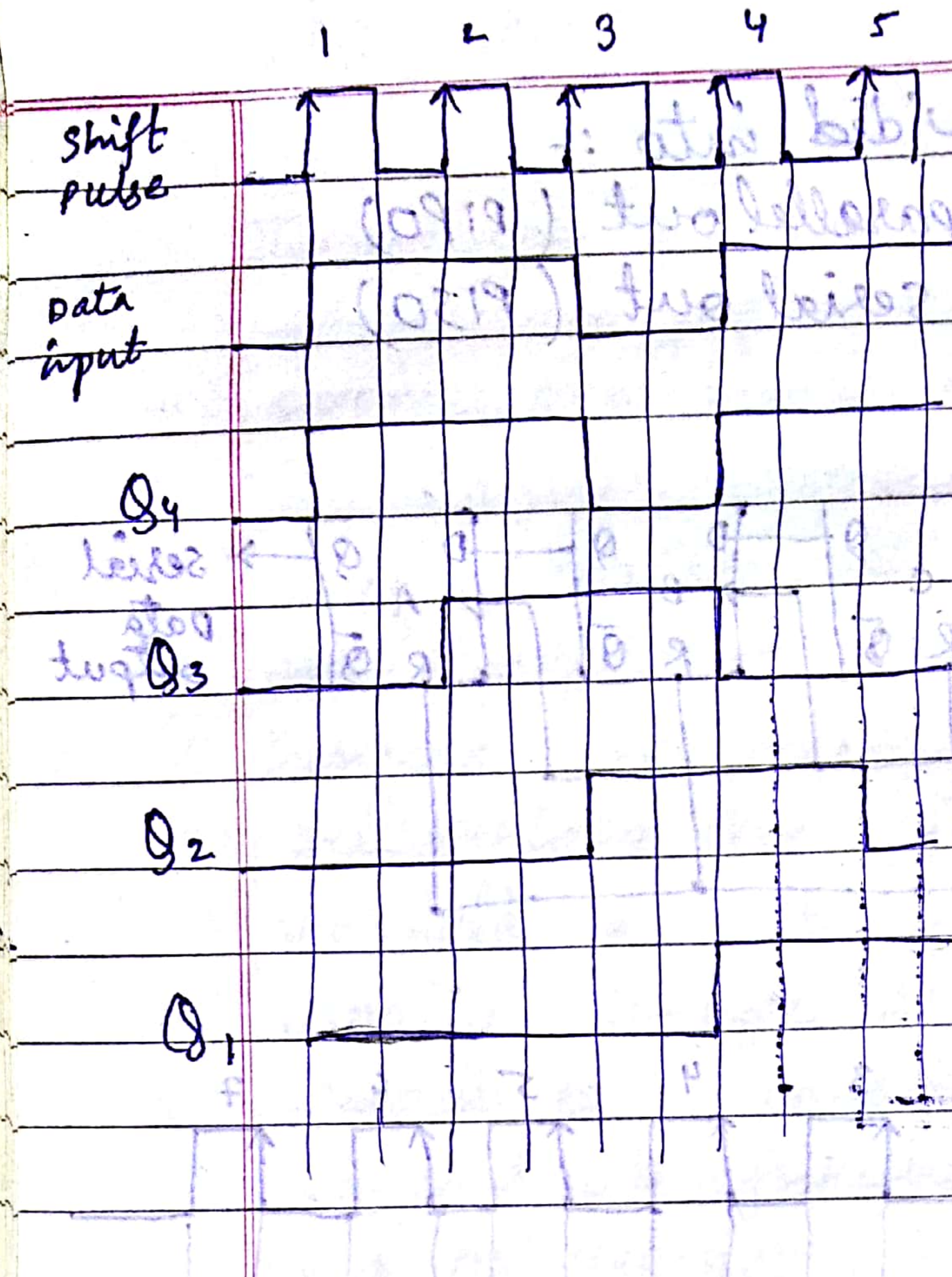


DELTA My NoteBook

Scanned by Imran Khalid

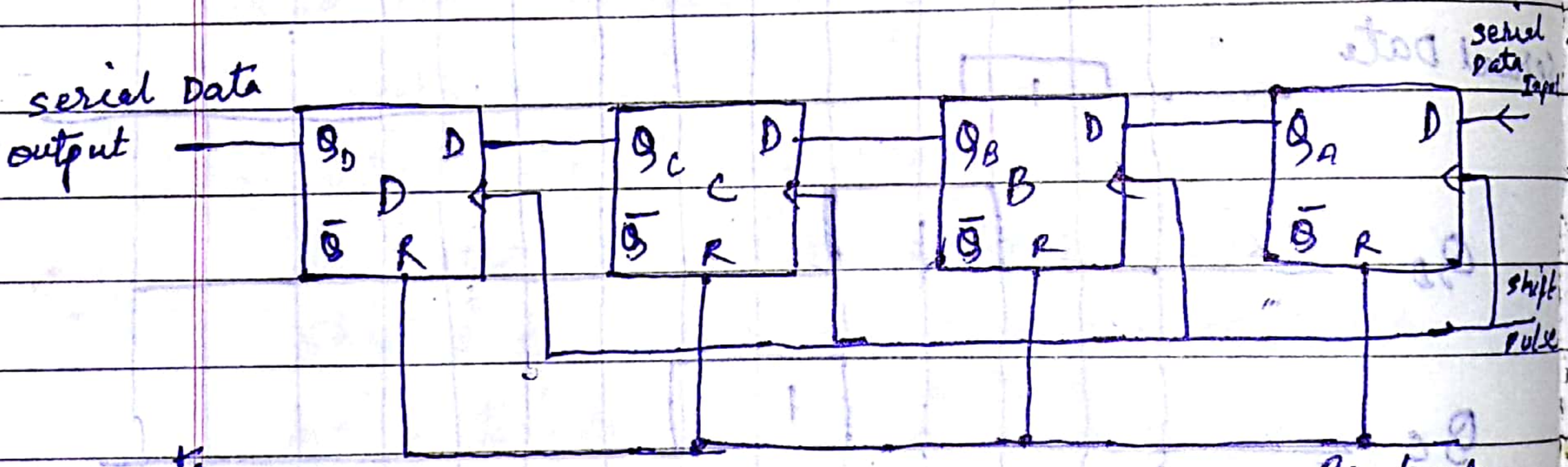
06/09/2016

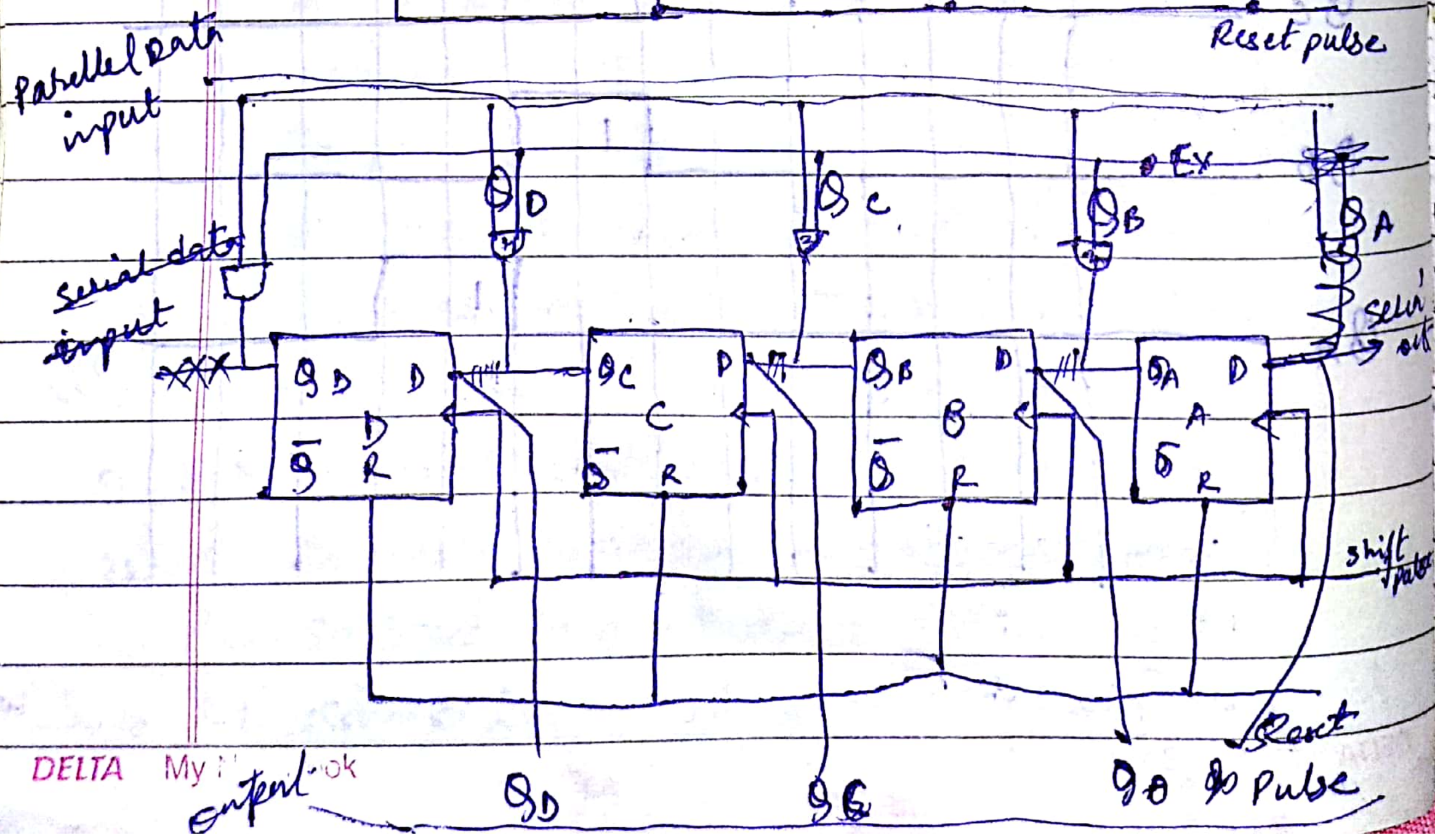
Page no.



(1101)

1	0	0	0
1	0	0	0
1	0	1	0
1	0	1	1



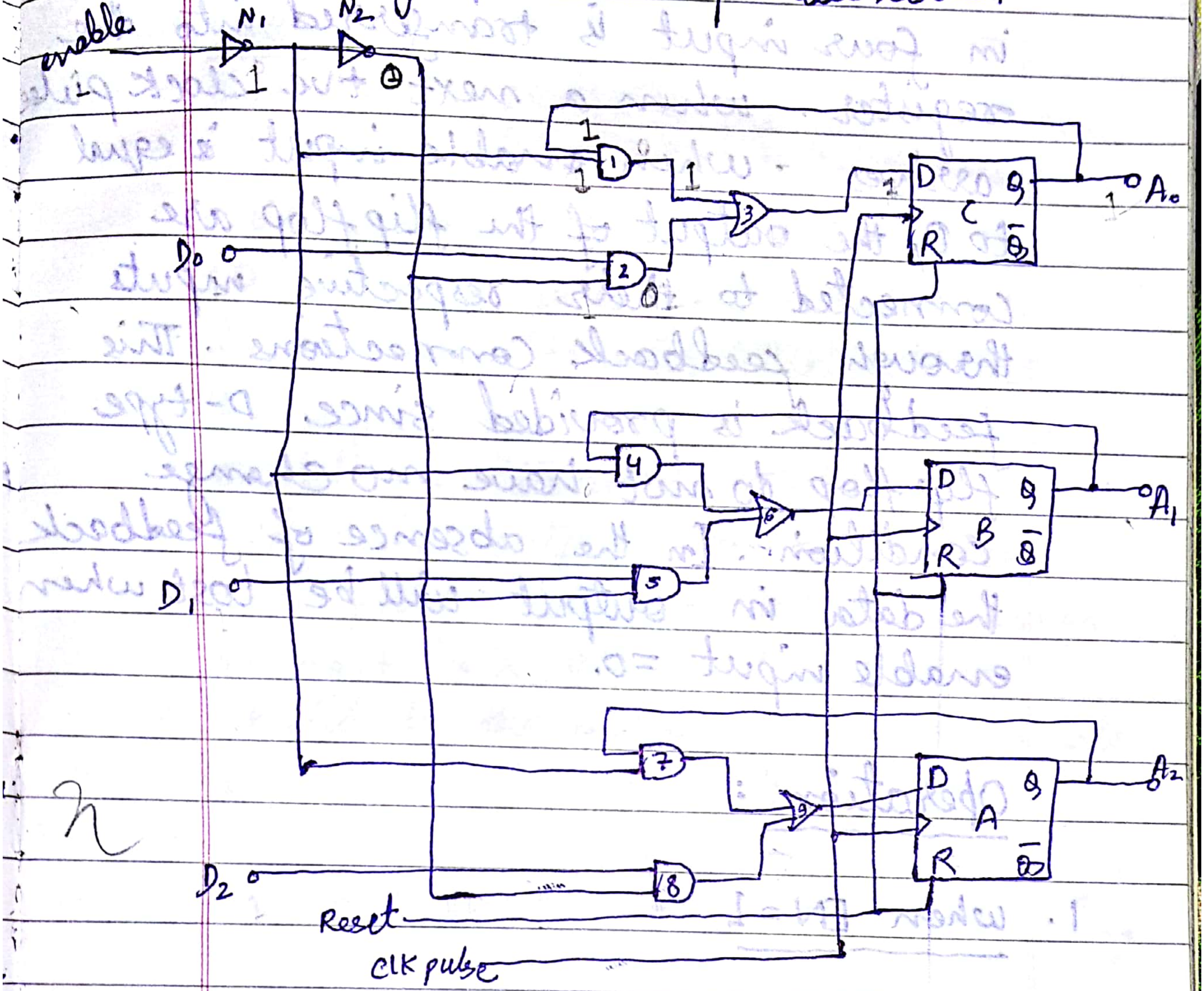


DELTA My Notebook

Scanned by Imran Khalid

PIPO

3 bit register with parallel load.



let $D_0 = 1$, $D_1 = 1$, $D_2 = 0$

As shown in the figure it consist of +ve edge operated · D-type connected to common clock shift pulse. The data to be transferred is applied in parallel to D input of the flip flop through a combination of AND or OR gates. AND enable input is used which decides of which +ve clock pulse the

Scanned by Imran Khalid

data is to be transferred. when the enable input = 1, the data in four input is transferred into the register. when a next +ve clock pulse arrives - when enable input is equal to 0, the output of the flip flop are connected to their respective inputs through feedback connections. This feedback is provided since D-type flip flop do not have no change condition. In the absence of feedback the data in output will be lost when enable input = 0.

Operation :

1. when EN = 1

let the data to be transferred D, $D_0 = 1$, $D_1 = 1$, $D_2 = 0$. Assuming all the output where at 0 due to some reset pulse, then input of gate 1, gate 4, gate 7 will be 00, then gate 2,5 will be (1,1) and input of gate 8 will be 01 these gates following their laws will transfer the data at the end of input C, B, A when a +ve clock pulse arrives these data will be transferred to their

Scanned by Imran Khalid

respective outputs A_0, A_1, A_2.

2. <u>when $E_N = 0$</u>

Then due to feedback the input of gate 1 & 4 will become (1,1), gate 2 & 5 will become (1,0) gate 7 will be (0,1). These gates following their laws will transfer the data at the input of C, B, and A. since enable is disabled. The register will held their output even when a +ve clock pulse arrives. In this way, when the next data arrives, it will be shifted to the output using the enable input.

Memory Devices

Storage of data is an essential for computer systems. Computers may use of memory devices to store data as well as make it available for processing when required.

Normally for storing bulk data computers make use of harddisk, magnetic tapes, floppies, pendrives etc. But memory requirement is not so large a bank of semiconductor devices or circuits are used to store data or serve as a memory device. There are two kinds of memory

(1) semiconductor memory (main)
(2) Magnetic memory (secondary)

- Semiconductor memories are fast, smaller and lighter and consume less power. They consist of a matrix of memory cells as a no. of digital circuits that provide different function such as address, seclection and the control. They are used as main memories of a computer.
- Magnetic memories are slow but cheaper than semiconductor memories.

DELTA My NoteBook

Scanned by Imran Khalid

19/09/2016

Page no.

They are used as secondary memories for bulk storage of data. secondary memories are classified as

1. RAM
2. ROM
3. PROM
4. EPROMs
5. EEPROMs (E^2PROM)

Memory cell

A memory cell is a device or an electrical ckt that is used for storing a single binary digit.
A memory unit is a collection of memory cells with associated ckt's to transfer information in and out of registers.
As shown in the diagram finally binary storage cell is a basic building block of a memory unit.
A memory unit will consist thousands of such cells. Each binary cell can store one bit of data. It consist of one flip flop R'S or JK and five gates arrange as shown in the fig. ! The cell has three inputs and one output terminal. The flip flop operates without a clock pulse because the purpose is to store information of the input in the binary cell.
The function of select input is to select one cell out of many cells available in a unit. The function of read write input is to perform read write operation. With Read/write = 1, the cells performs Read operation & R/w=0, the cells performs write

DELTA My NoteBook

Scanned by Imran Khalid

19/07/16

Page no.

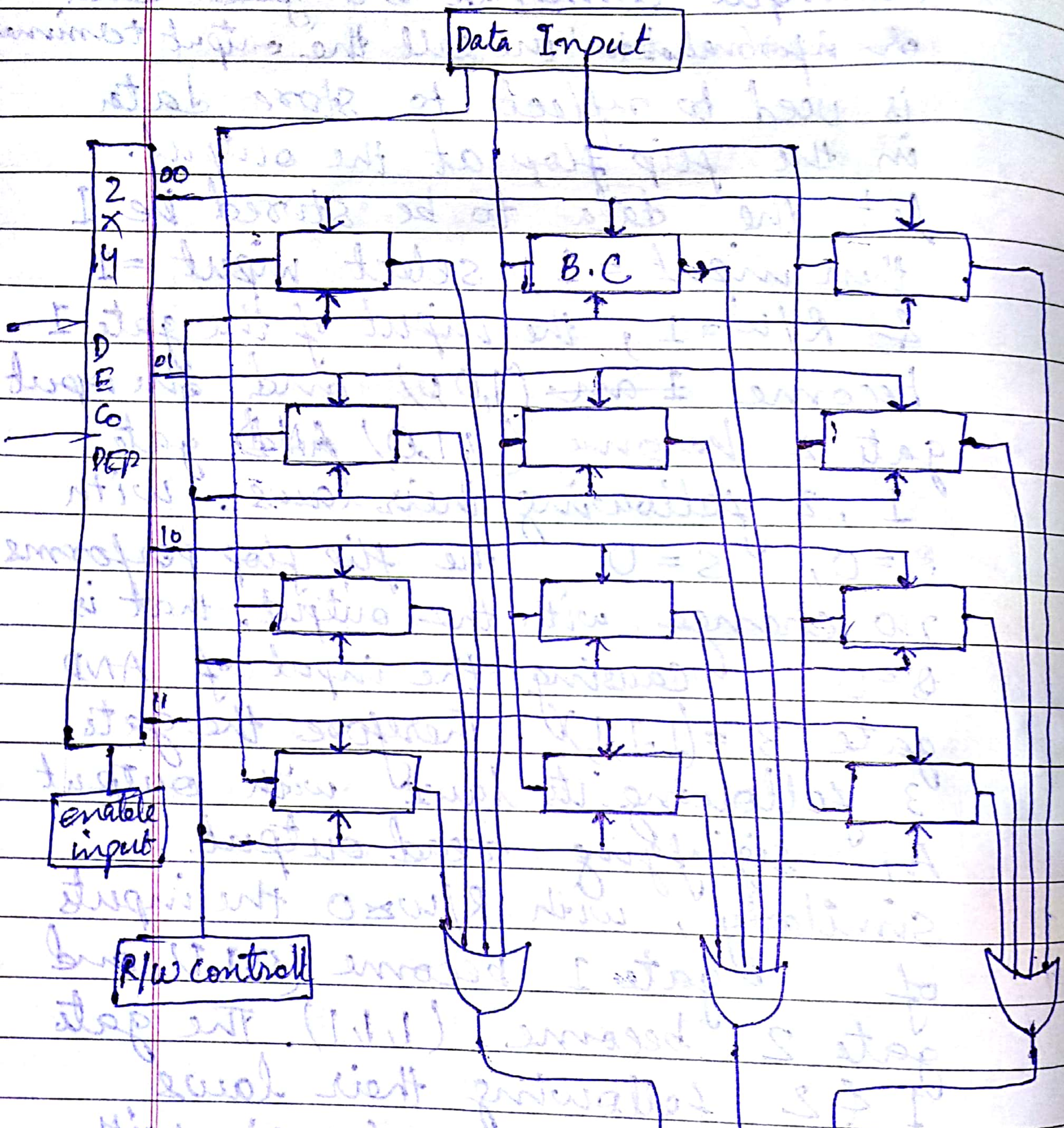
operation.

The input terminal is to feed data or information to the cell the output terminal is used to reflect to store data in the flip flop at the output. let the data to be stored be 1 then input = 1, select input = 1 & R/W = 1, the input of the gate 1 become ~~1 and~~ (1,0,0) and the input gate 2 become (1,1,0) ~~AND~~ gate 1, 2 following their laws. with R = 0, S = 0 the flip flop performe no change with the output, that is Q = 0 causing the input of AND gate 3 = (1,1,1). Therefore the gate 3 following its laws with output A, signifying read output.

Similarly, with R/W = 0 the inputs of gate 1 become (0,1,1) and gate 2 become (1,1,1). The gate 1 & 2 following their laws will output ~~zero~~ (0,1). with S = 0 1 and R = 0 the flip flop move into set state that is Q = 1, $\bar{Q}$ = 0. This makes the input of gate 3 as (1,0,0) which signifies write operation.

Scanned by Imran Khalid

4x3 I.C. RAM



This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

It consists of 4 words of three bit each and has a total of 12 binary storage cells as shown in the figure. Each block contains within it the CKt. of memory cell. It also consist of a two into four with an enable input. The decoders carries two address inputs which go through the decoder to select one of the four word. Once a word is selected read write input determines the operation and the output can be had at the output of three OR Gates.

With enable input = 0 all the outputs of the decoder become zero and non-of the memory word is selected.

with enable input = 1, one of the four words is selected depending on the bit combination of the two address line.

with red-write control = 1, the bits of the selected word will produce o/p = 1 of the input of three gates. The ~~most~~ most selected binary cell will produce zero o/p in the inputs of three

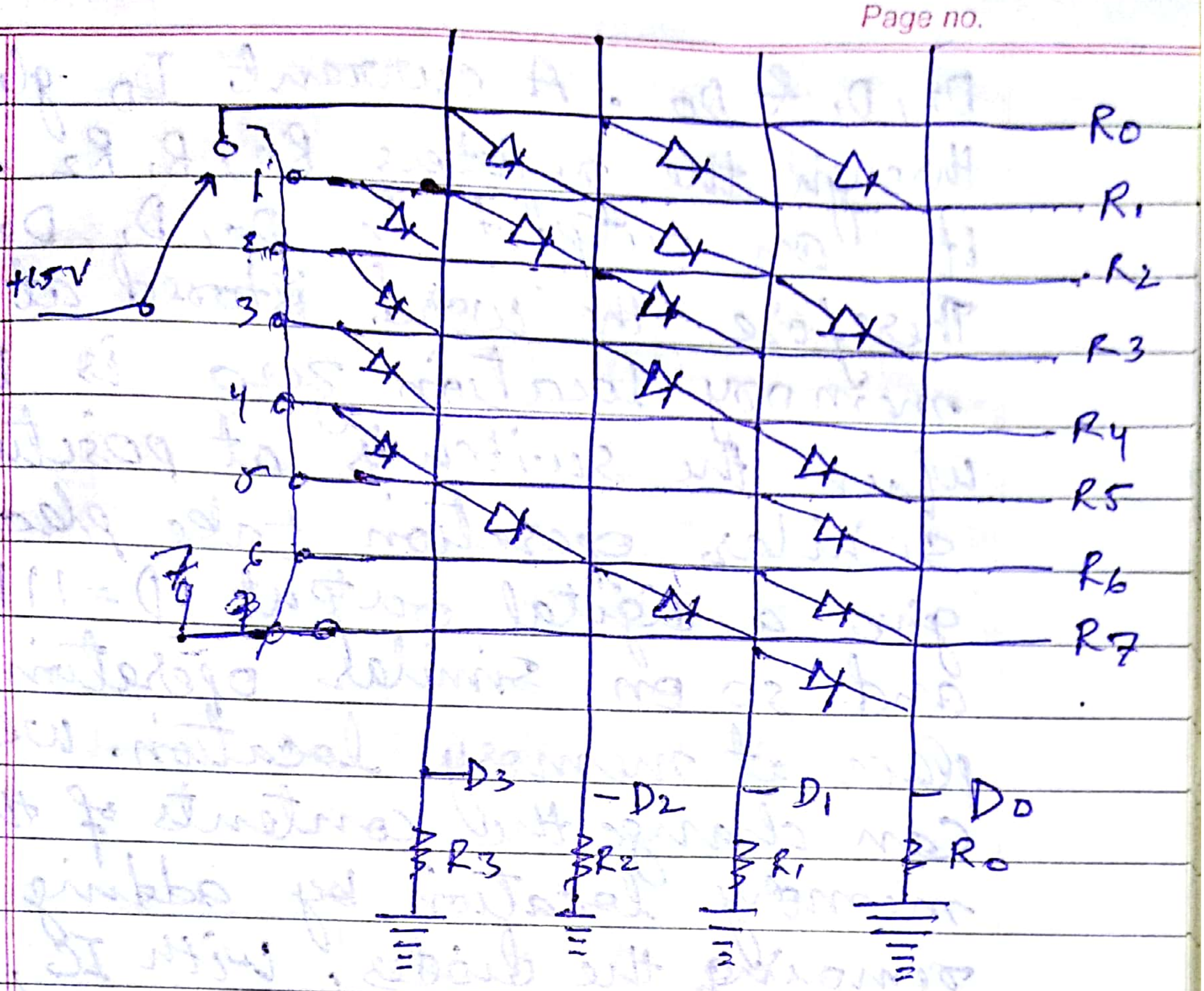
DELTA My NoteBook

Scanned by Imran Khalid

OR gates. Resulting in and output = 111.
with R/w control = 0, information available in the data inputs lines is transferred into the flip flop of the selected word (i.e, non selected binary cell are disabled by their selection lines go so their previous values remain unchanged.
Therefore with memory enabled = 1 the R/w control initiates the R/w operations. And in Inhibit operation is obtained by putting memory enabled = 0. This leaves the content of all words in memory as they left in respective of the value of R/w control

Read Only Memory (ROM)

Organization



$R_0 - R_7 \Rightarrow$ Registers

$+5V \Rightarrow$ logic 1

$0 \; -5V \Rightarrow$ logic 0

In the above figure, each horizontal Row is a register or a memory location The line R_0, R_1, R_2 has three registers whereas The line RR_2 and soon are two. arranged in a particular manner as shown in the figure. The output of the ROM is a digital word

$D = D_3 D_2 D_1 D_0$.

when the switch is at zero position +ve 5 volt turns ON the diode

DELTA My NoteBook

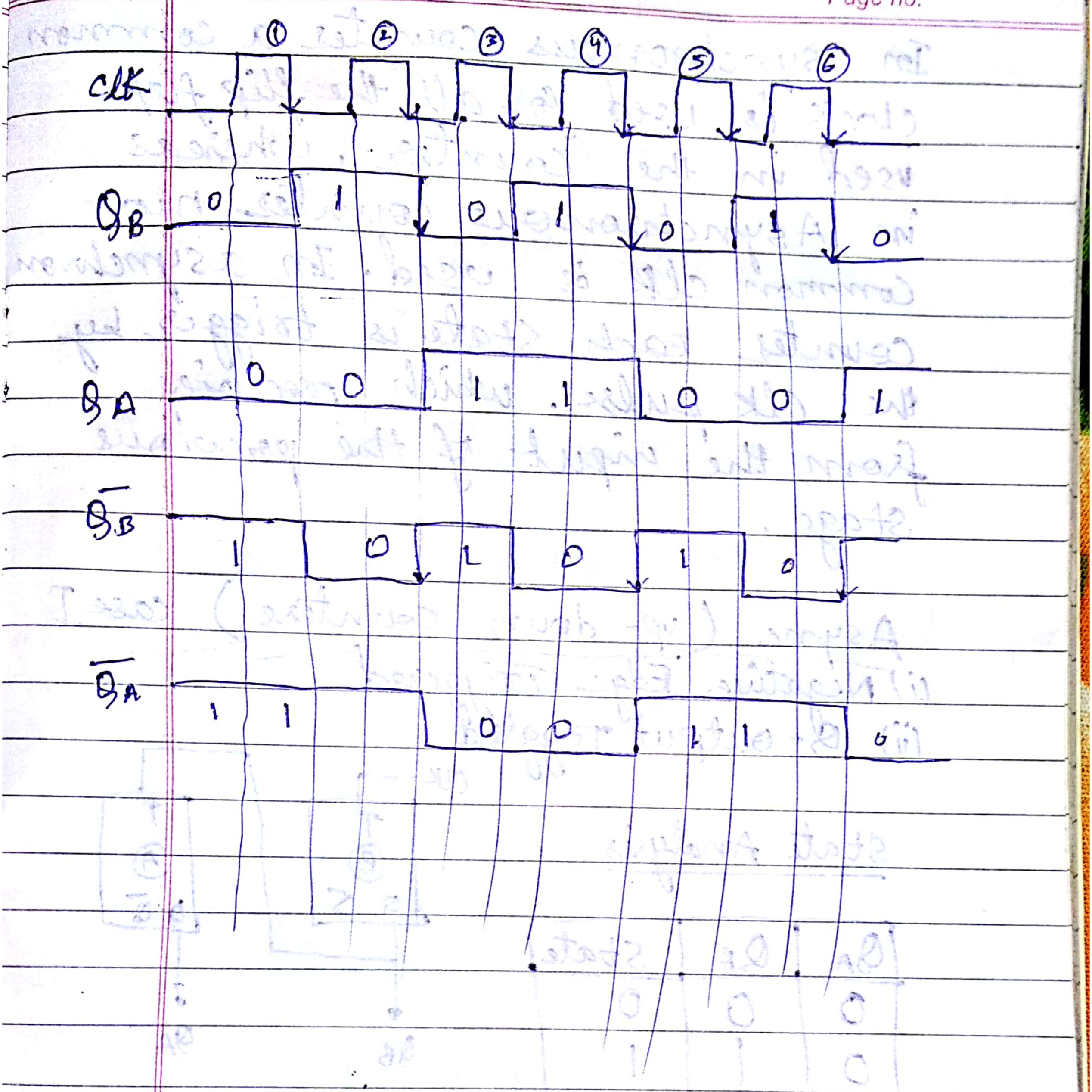
Scanned by Imran Khalid

Page no.

D_2, D_1 & D_0. A current I_D glows through the registers R_0, R_1 R_2 resulting it an output in D_0, D_1, D_2. Therefore the word stored at memory location zero is D = 0111. When the switch is at position I, similar operation take place to give a digital output D = 1110, and so on. Similar operation take place at memory location. We can change the contents of the memory location by adding or removing the diodes. With IC, the manufacturer stores the word at the time of fabrication.

22/Sep/2016

Page no.



A counter that uses T type flipflop and some combinational element to perform the counting function such that the output of one is used as clock input to the other flip flop. Counters are divided into two major categories

① Asynchronous or ripple counter

② synchronous or parallel counter

DELTA My NoteBook

Scanned by Imran Khalid

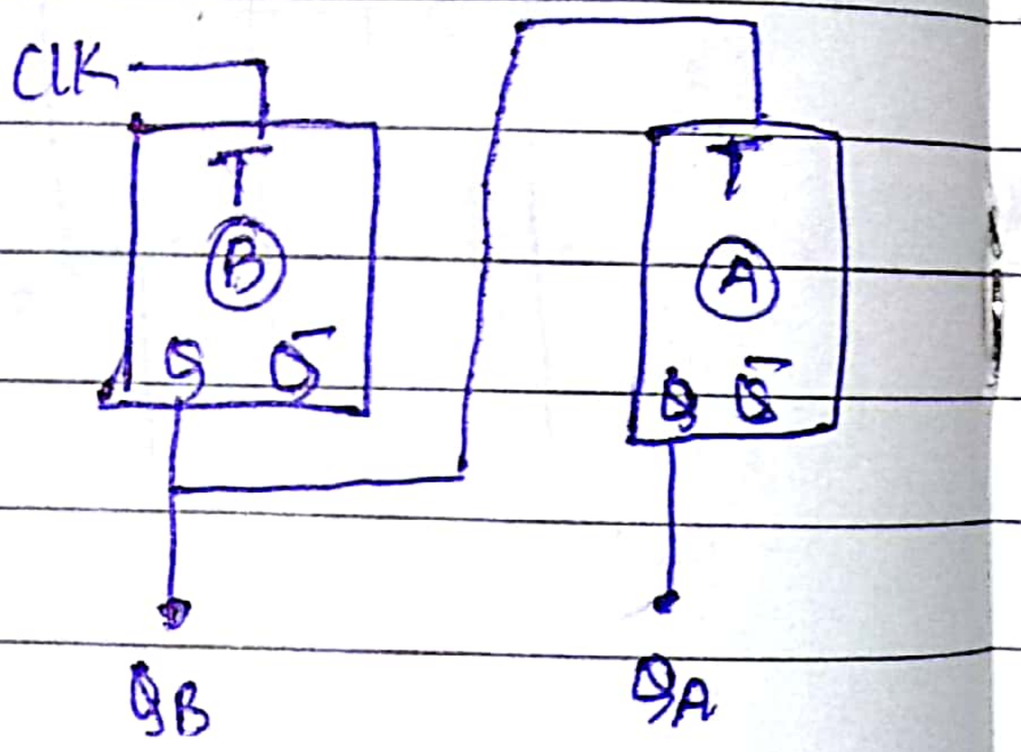
Page no.

In synchronous counter a common clock is used for all the flip flop used in the counter, whereas in Asynchronous counter no-Common clk is used. In asynchron counter each state is trigger by the clk pulse. which receive from the input of the previous stage.

Async (up-down counters) case I

(i) Negative Edge Triggered

(ii) $\bar{Q}$-output Toggled



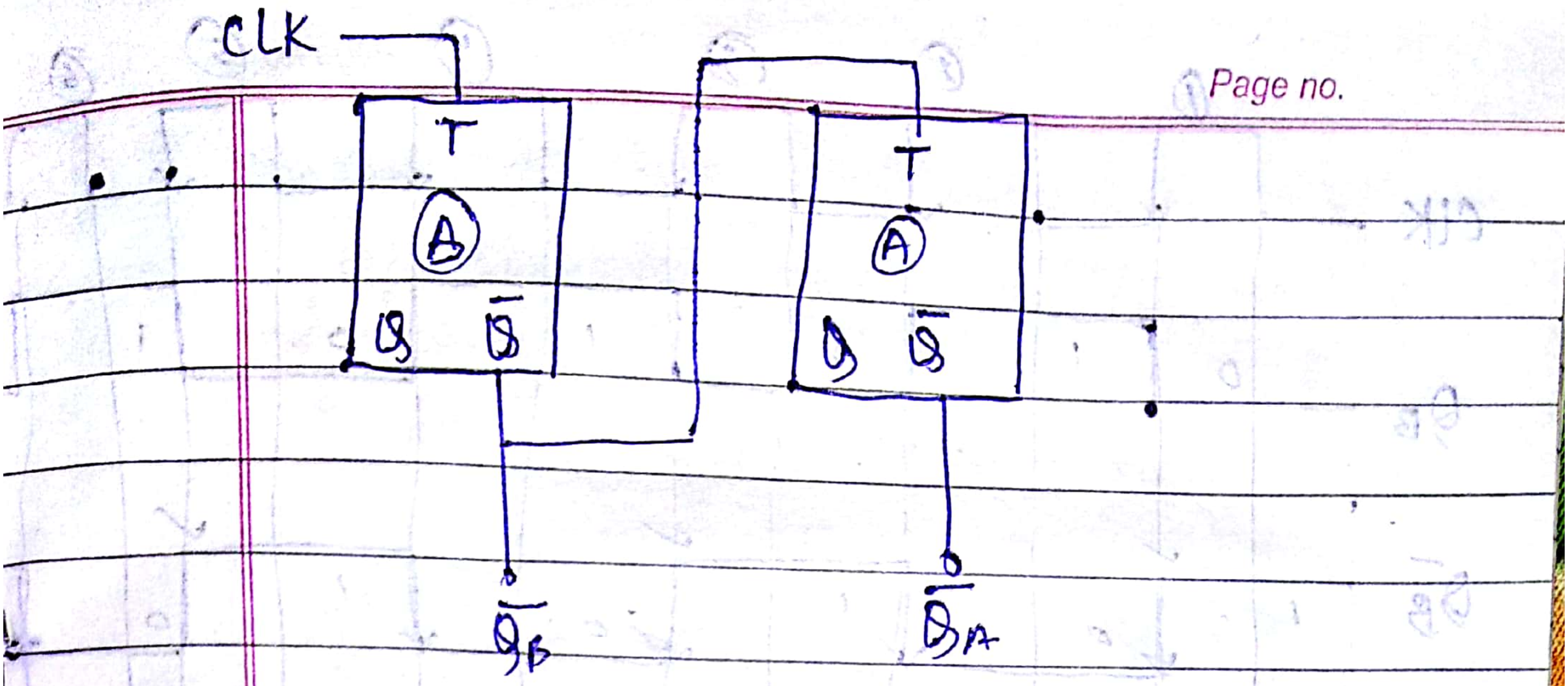
State Analysis

Q_A	Q_B	state
0	0	0
0	1	1
1	0	2
1	1	3
0	0	0
0	1	1

Up Counter

Scanned by Imran Khalid

22/09/2016

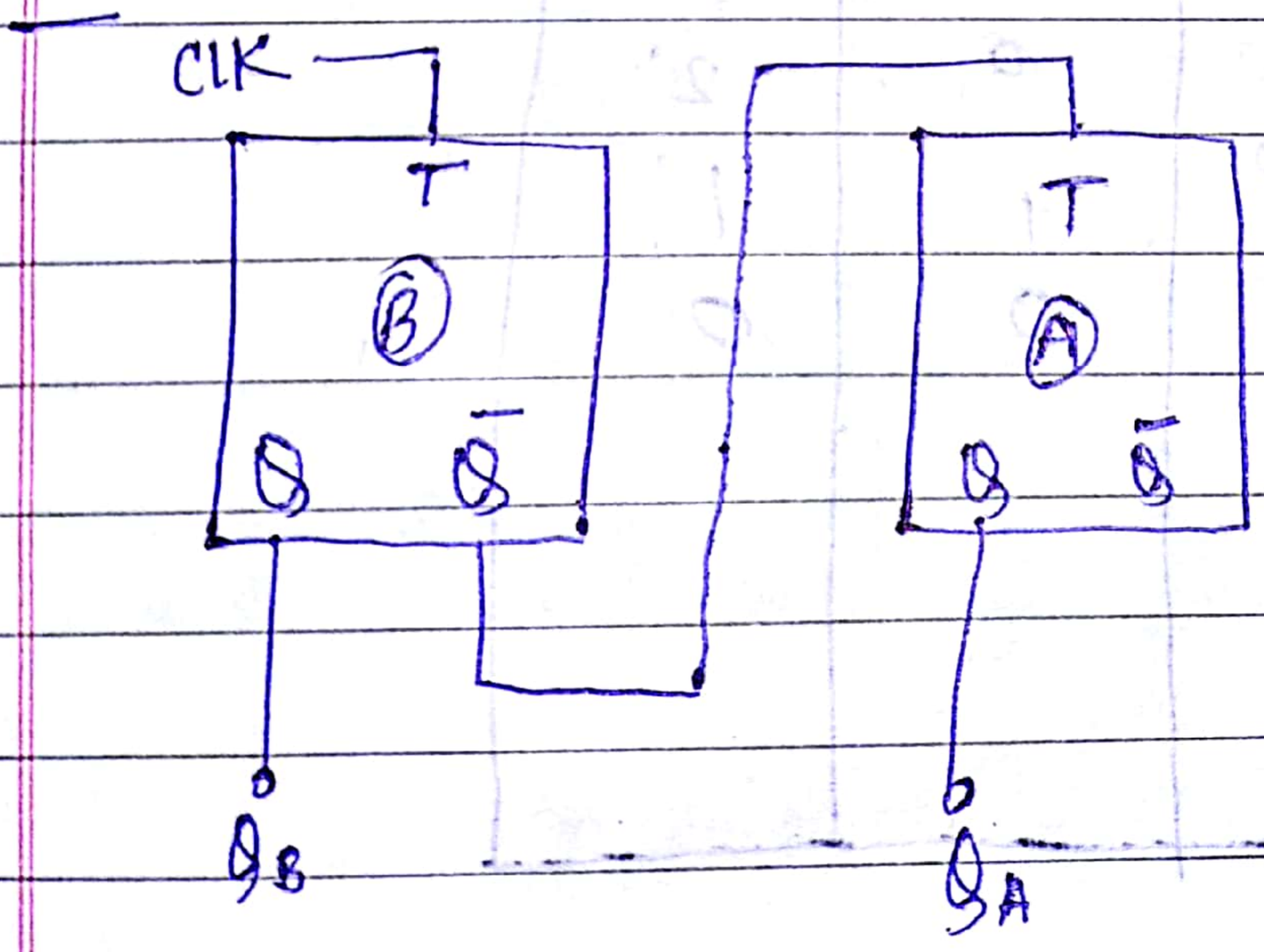


State Analysis

$\bar{Q}_A$	$\bar{Q}_B$	State
1	1	3
1	0	2
0	1	1
0	0	0
1	1	3

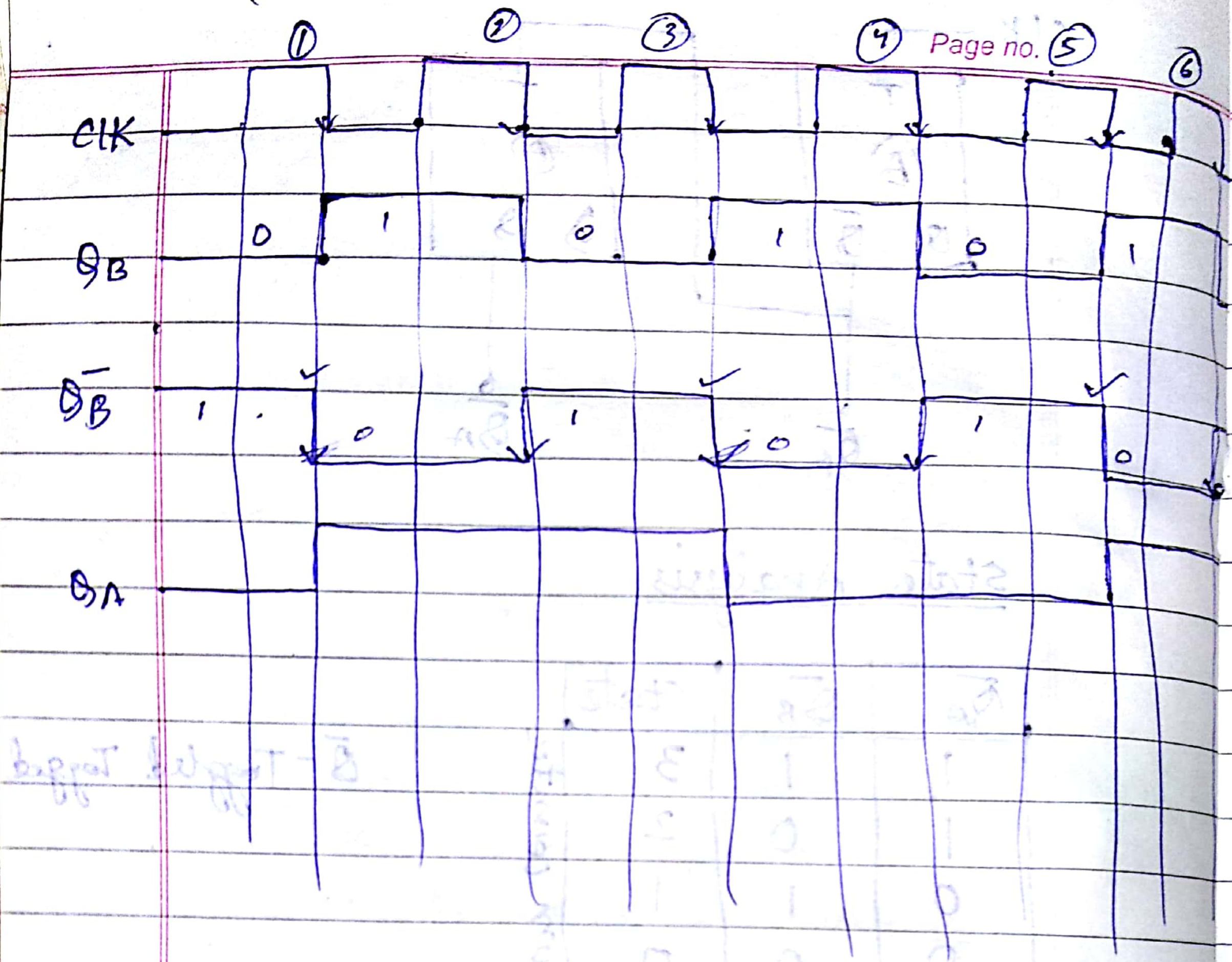
Down counter

$\bar{Q}$ - Toggled Togged



DELTA My NoteBook

Scanned by Imran Khalid



Q_A	Q_B	state
1	1	3
1	0	2
0	1	1
0	0	0

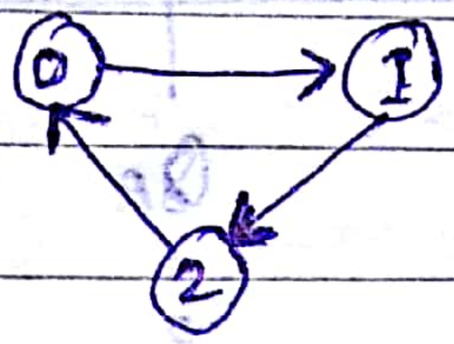
Scanned by Imran Khalid

04/10/2016

Page no. II

Q → Design a 2 output toggled modulo 3 up counter. The counter is -ve edge triggred and have reset input

State Diagram



Max. Countable NO. = 2

Binary eq. of 2 = 10

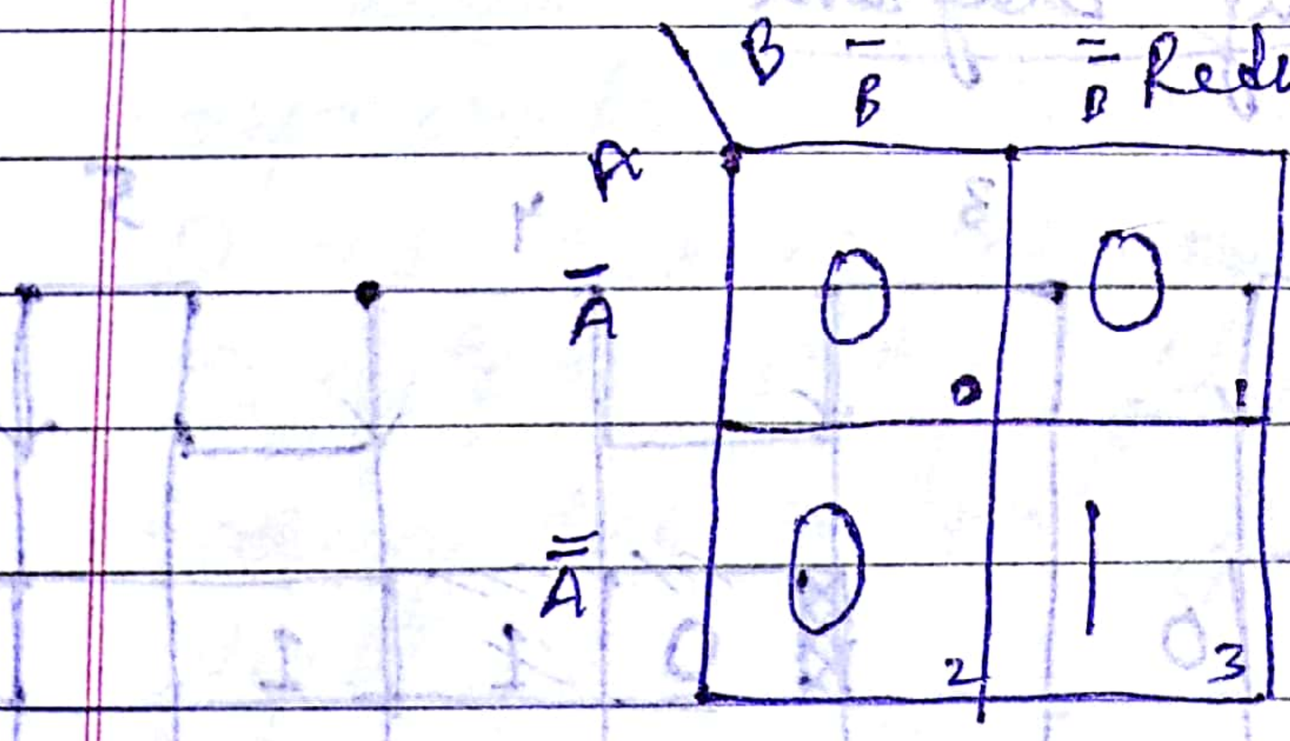
No. of variable = 2

No. of flip flop = 2

No. of square K-Map = $2^n = 2^2 = 4$

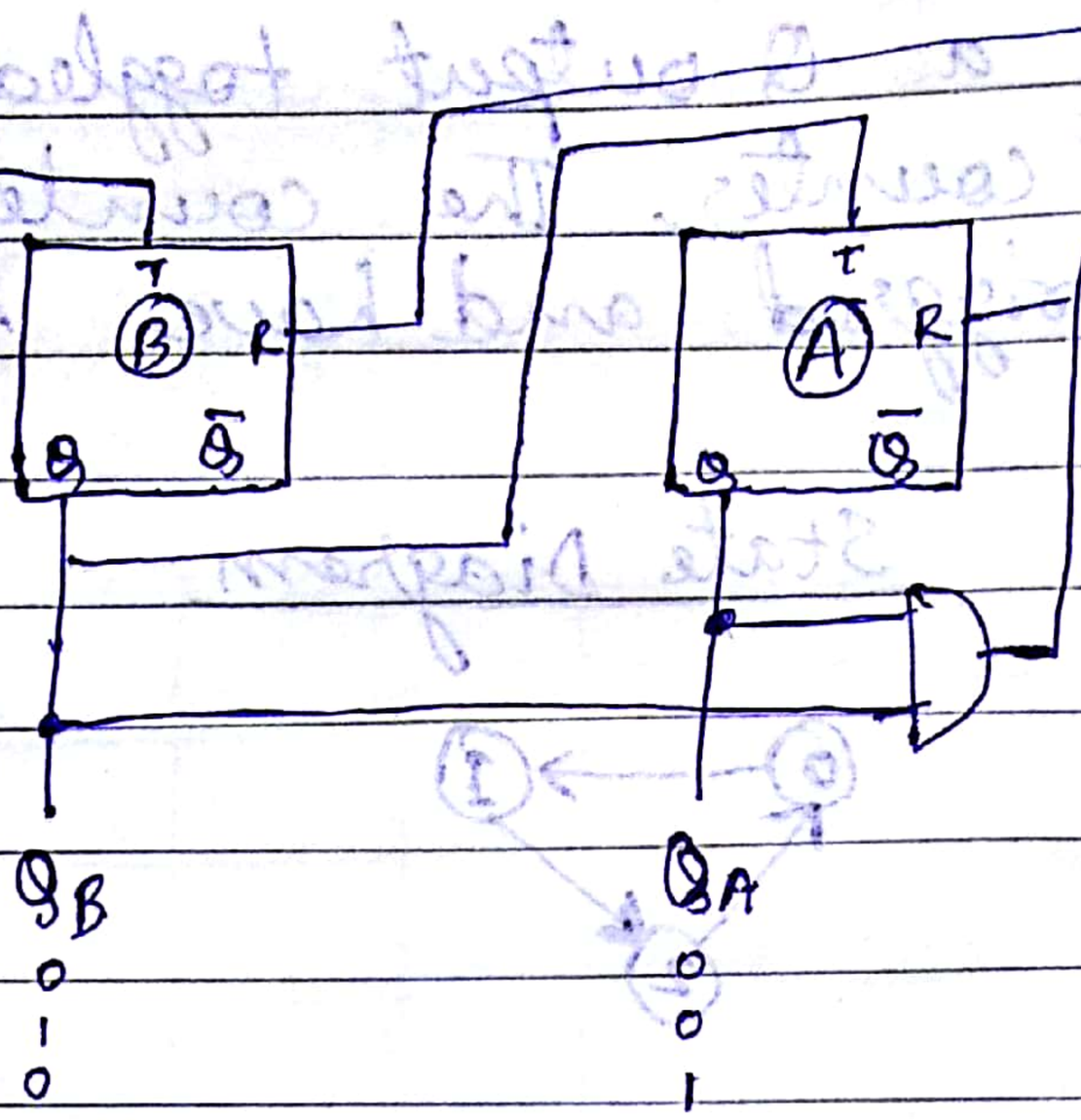
state to be detected = (3)

Reducing the Map



$Y = A.B$

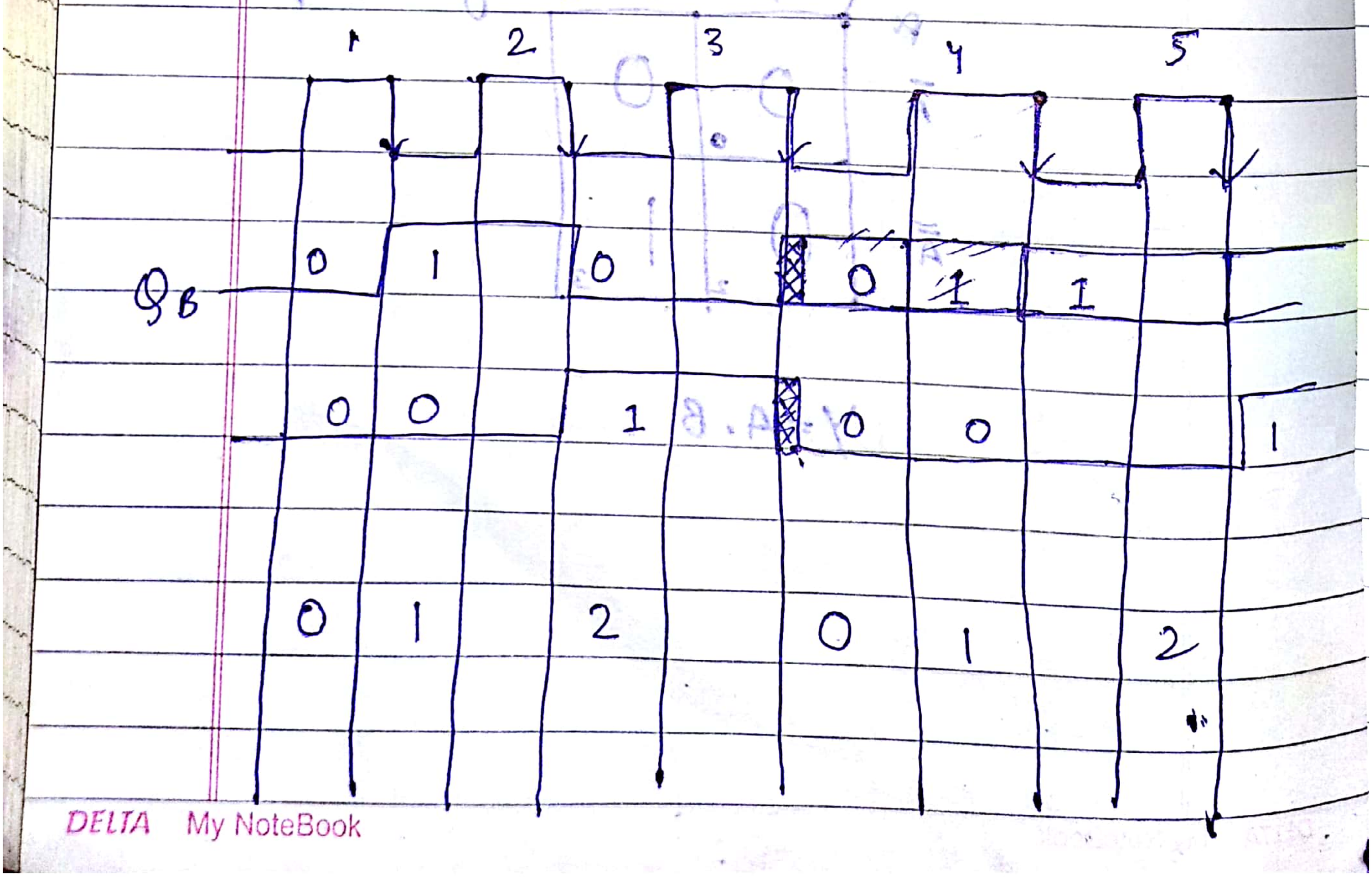
Scanned by Imran Khalid



State Analyses

Q_A	Q_B	State	
0	0	0	
0	1	1	
1	0	2	
1	1	3	R

Timing Diagram



DELTA My NoteBook

Scanned by Imran Khalid

05/10/16

Page no.

Q → Design a modulo 8 down counter. +ve edge triggered.

Q → Design a modulo 5 down counter, that toggles on -ve to +ve transition. Have toggled and have reset input. It should be a down counter.

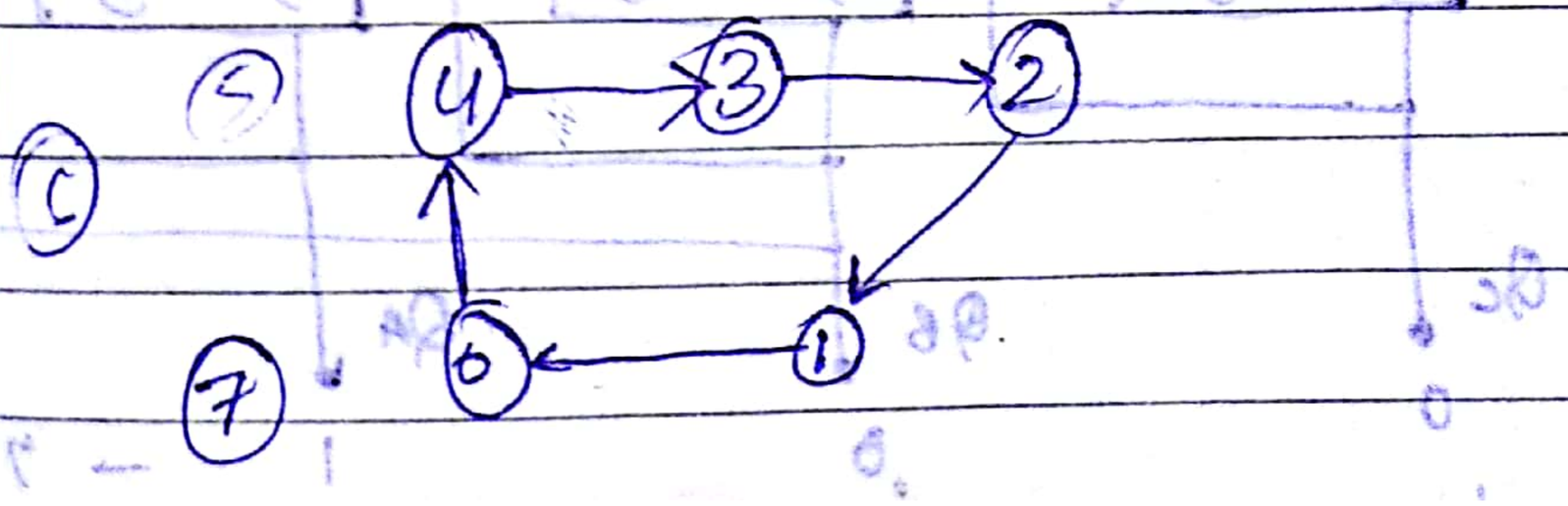
sol. $up = P_N \oplus Q_t \oplus Q$

where if $up = 1$ represent an up counter, if $up = 0$ represent down counter.

$P_N \Rightarrow$ if $P_N = 1$ represent +ve to -ve transition 0, represent -ve to +ve transition. $Q_t = 1$ represent toggling from Q output of the flip flop. $Q_t = 0$ represents $\bar{Q}$ output of the flip flop.

$Q = 1$ taking the output from Q output of the flip flop. $Q = 0$, taking the output from $\bar{Q}$ of the flip flop.

State Diagram



Scanned by Imran Khalid

Page no.

Max. countable NO = 4

Binary = 100

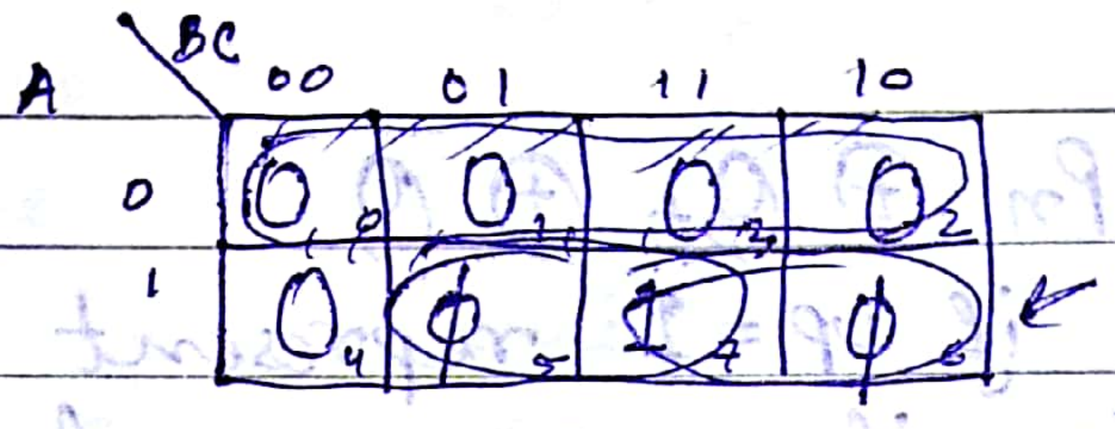
No. of variable = 3

No. of flip flop = 3

No. of square K-map = $2^n = 8$

State to be detected = 7

Dont. care state = 6, 5



$Y = A$ $\quad Y_1 = A(\bar{B}C + BC) = AC$

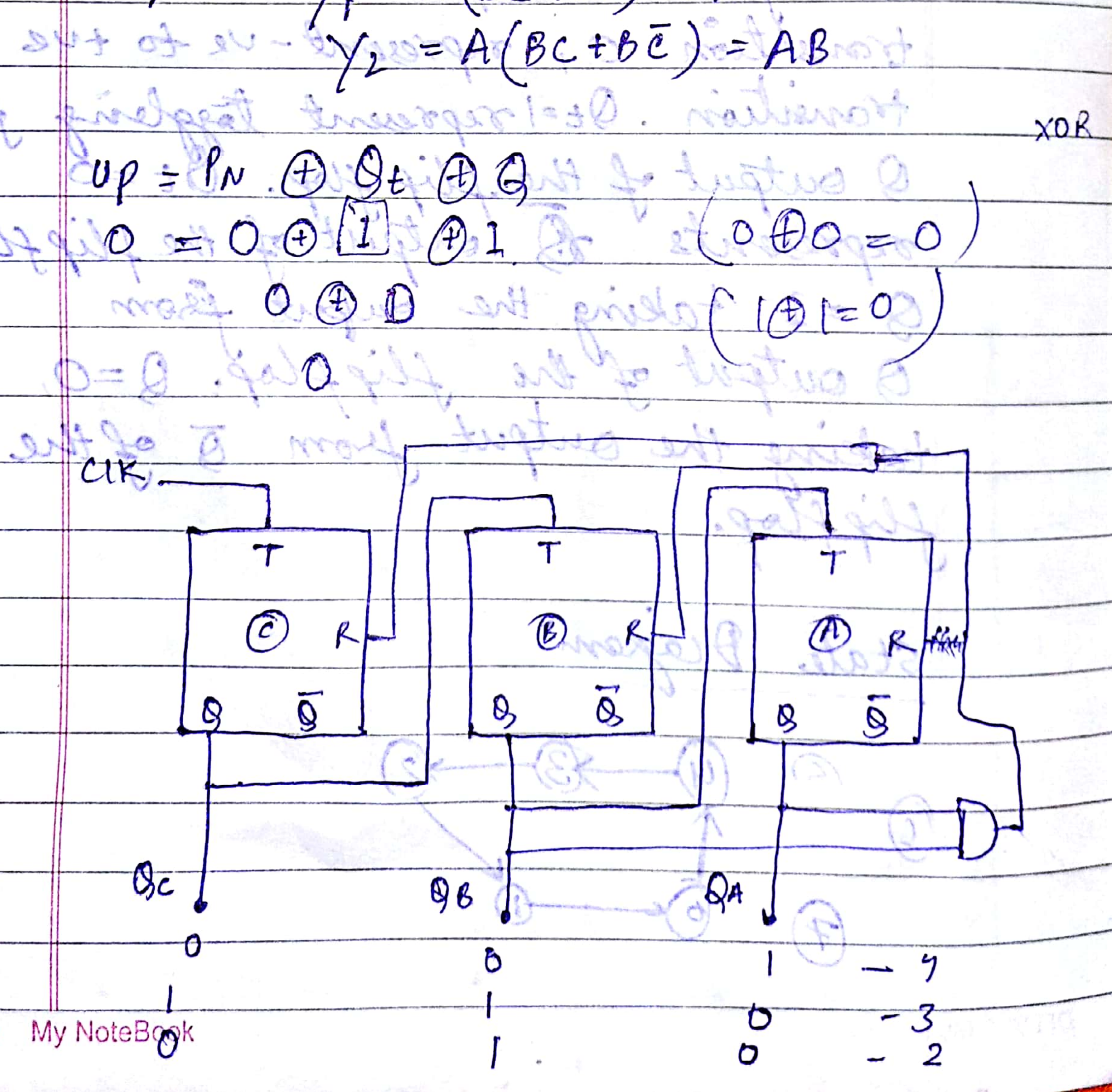
$Y_2 = A(BC + B\bar{C}) = AB$

XOR

$Up = P_N \oplus Q_t \oplus Q$

L.H.S → $0 = 0 \oplus 1 \oplus 1 \quad (0 \oplus 0 = 0)$

$0 \oplus 0 \quad (1 \oplus 1 = 0)$



DELTA My NoteBook

Scanned by Imran Khalid

Page no.

State Analysis

Q_A	Q_B	Q_C	State
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

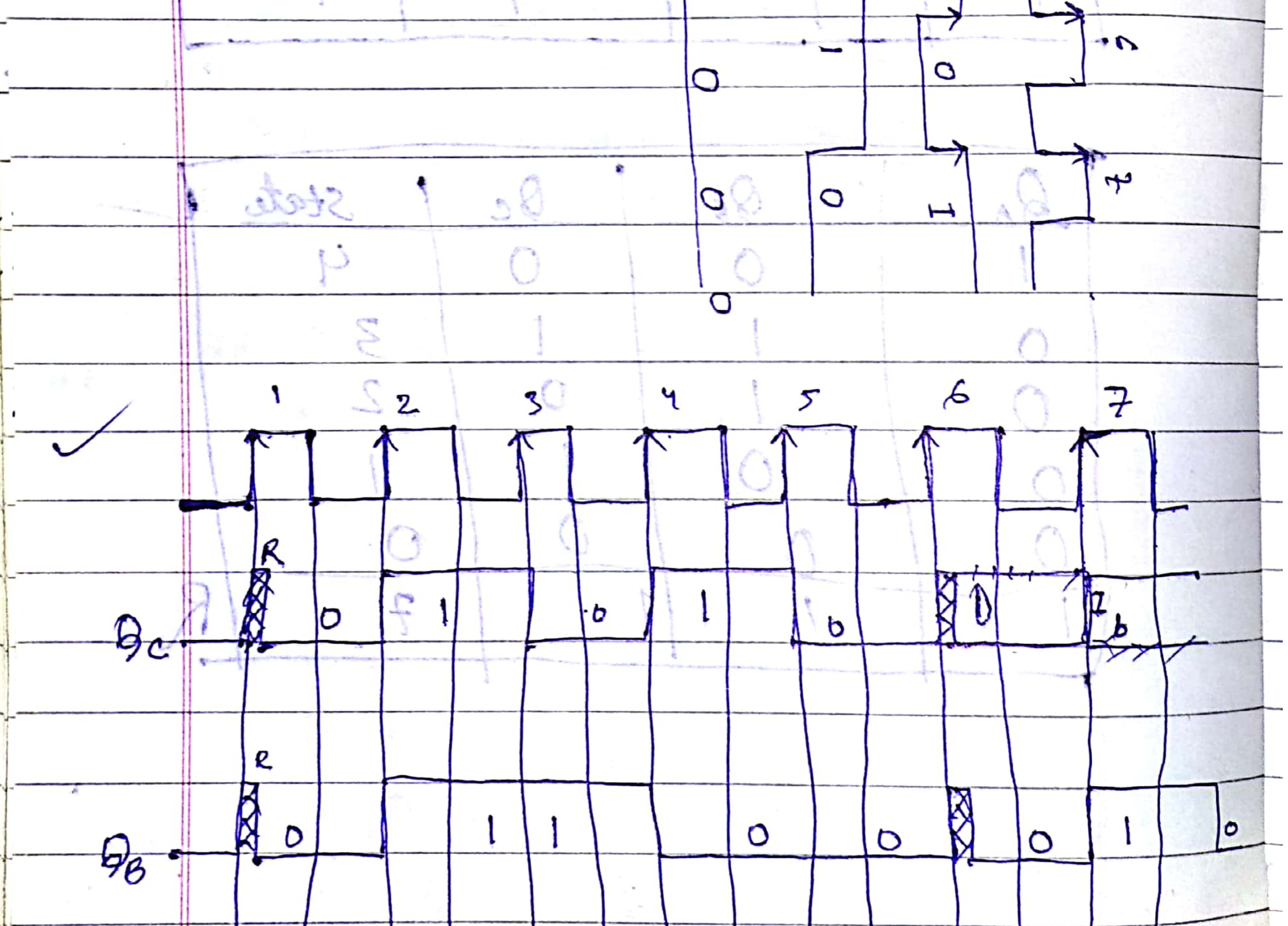
Q_A	Q_B	Q_C	State
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0
1	0	1	5
1	1	1	7
1	1	0	6

DELTA My NoteBook

Scanned by Imran Khalid

Page no.

Normal operation	Q_C	Q_B	Q_A	State
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7



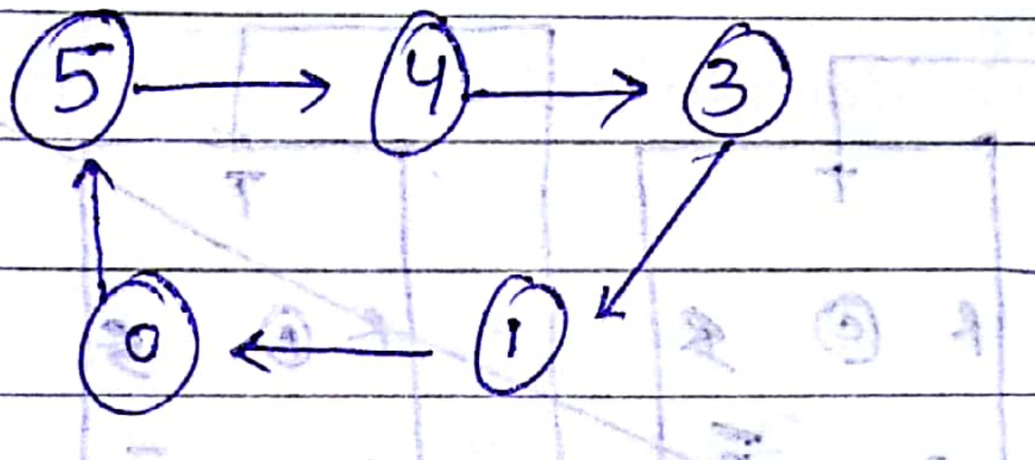
DELTA My Notebook

Scanned by Imran Khalid

06/10/2015

Page no.

Q→ Design a modulo 5 counter using flip flop that toggled on -ve to +ve transition and have toggled, set & Reset inputs the counter should be a down counter and must countdown the states 5, 4, 3, 1, 0.



Max. countable no. 5

Binary eq. = 101

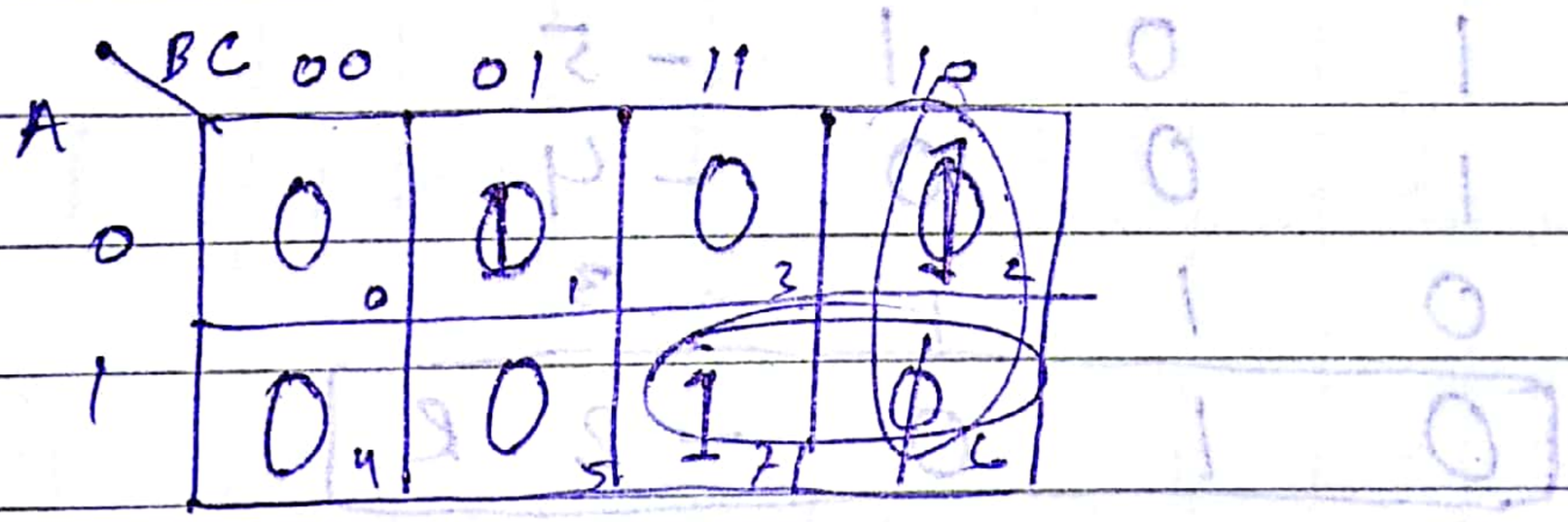
No. of variable = 3

No. flip flop = 3

No. of square = 8

State to be detected = 2, 7

don't care = 6



$Y = ABC + A B\bar{C} = AB$

$= \cancel{A}B\bar{C} + \cancel{A}BC = B\bar{C}$

$B\bar{C}\bar{A} + B\bar{C}A = B\bar{C}$

DELTA My NoteBook

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

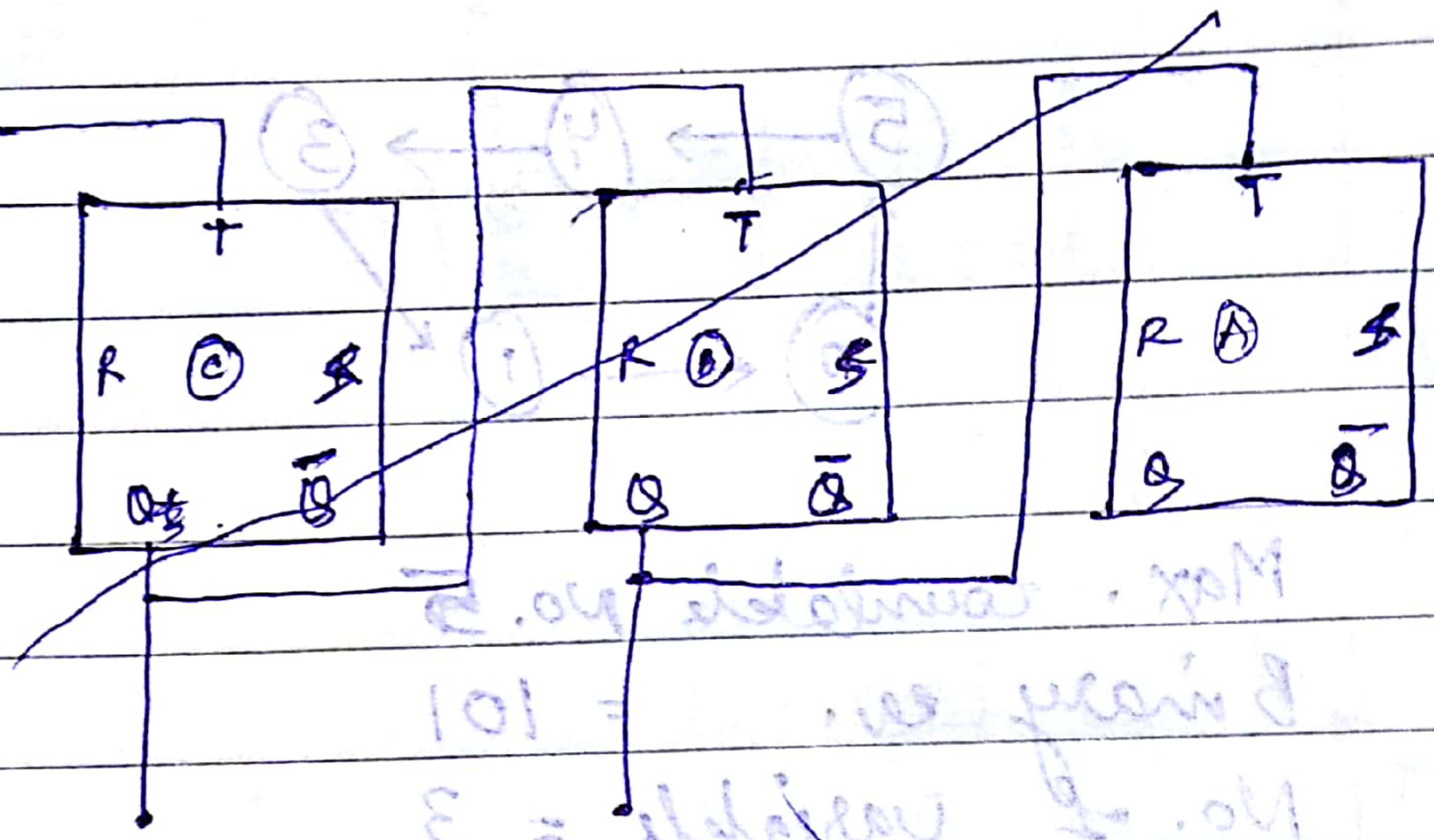
Page no.

$J_A = 1$ $K_A = 1$

$J_B = Q_C$ $K_B = Q_C$

$J_C = \bar{Q}_B$ $K_C = 1$

CLK



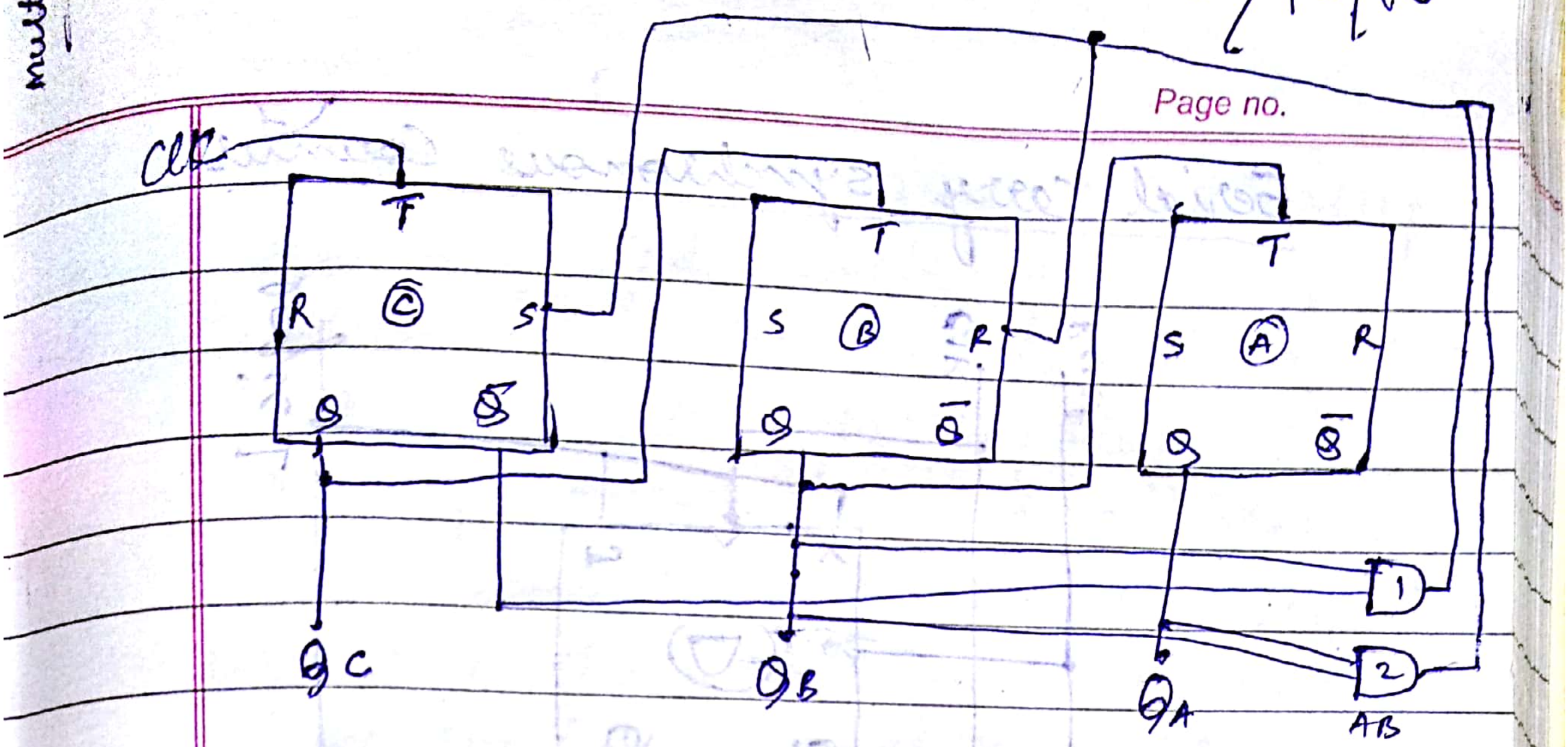
State Analysis

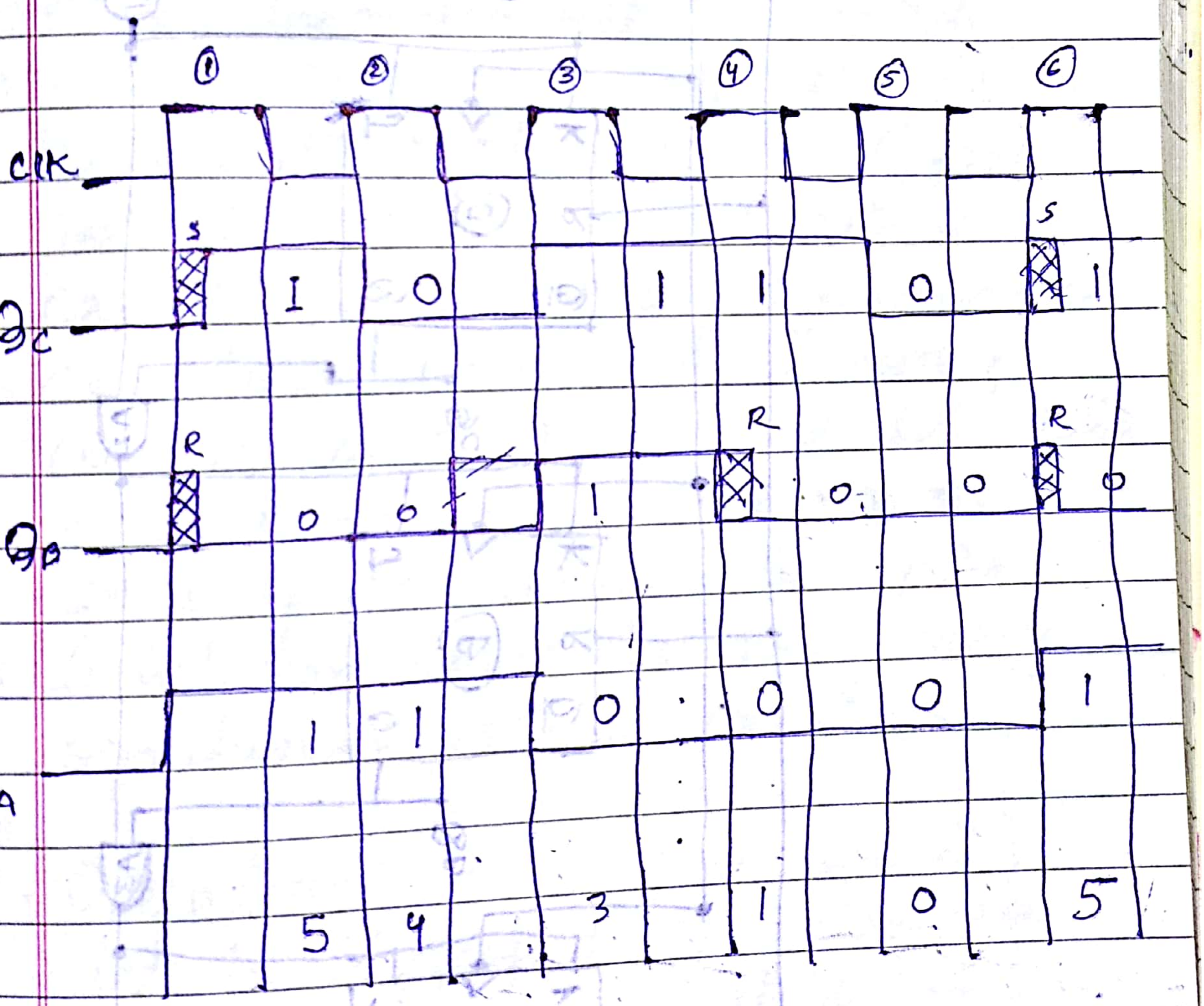
Q_A	Q_B	Q_C	
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2 R
0	0	1	1
0	0	0	0
1	1	1	7 R

Multivibrator

13/10/16

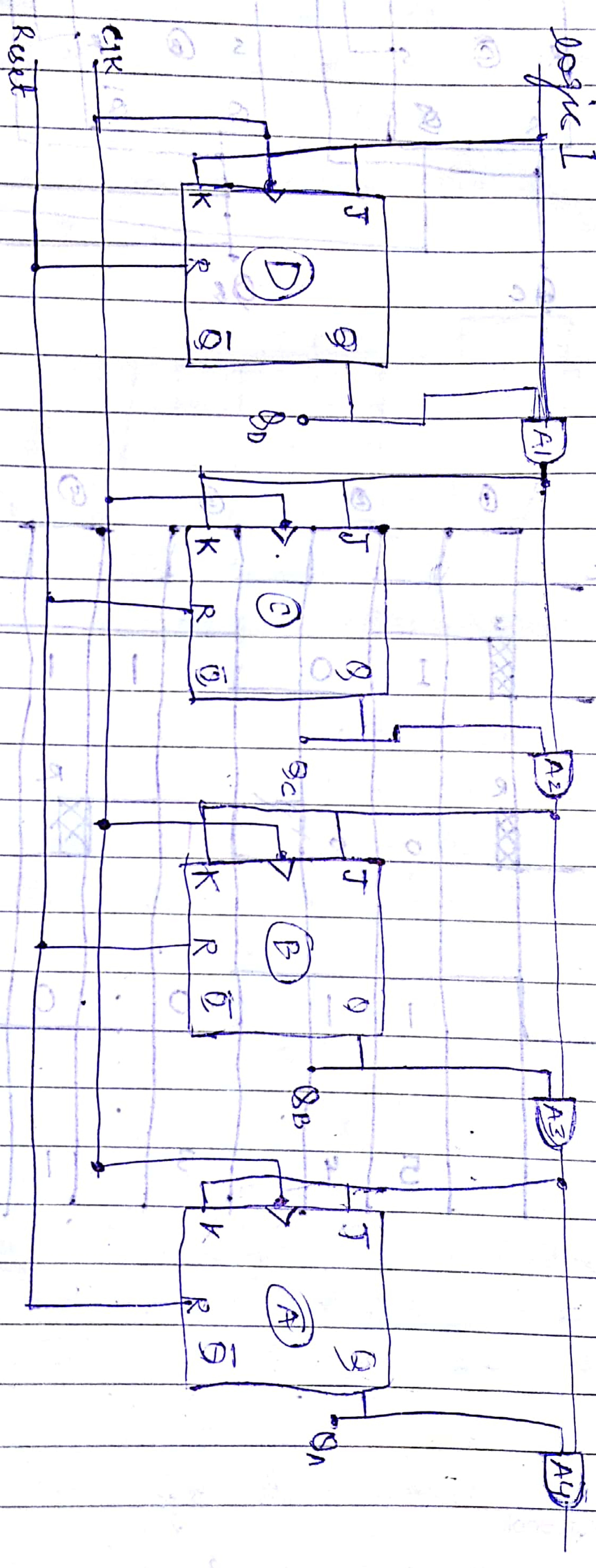
Page no.





Scanned by Imran Khalid

Serial carry synchronous Counters



4 bit Modulo 16 sync counter

As shown in the figure the flip-flop are connected such that they work in toggle mode i.e., J = K = 1. Also the flip flop are -ve edge triggered. and connected to common clock pulse therefore whenever the clock pulse changes from +ve to -ve all the flip flops change their state simultaneously. Since the information regarding the state of previous flip flop is carried to successive flip flop through a series of AND Gate it is called serial carry synchronous Counter. However this type of Counter also has speed limitation of its own due to the use of a series of AND Gates. This speed limitation is rectified by using synchronous parallel counter.

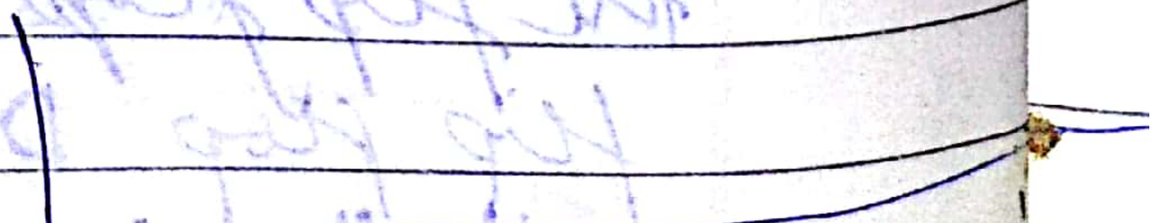
Operation

let the flipflop be connected to a common clock pulse. let due to some reset pulse the output of the flip flops be at 0. except flip flop D, which is at logic 1. all the inputs of remaining flip-flop

DELTA My NoteBook

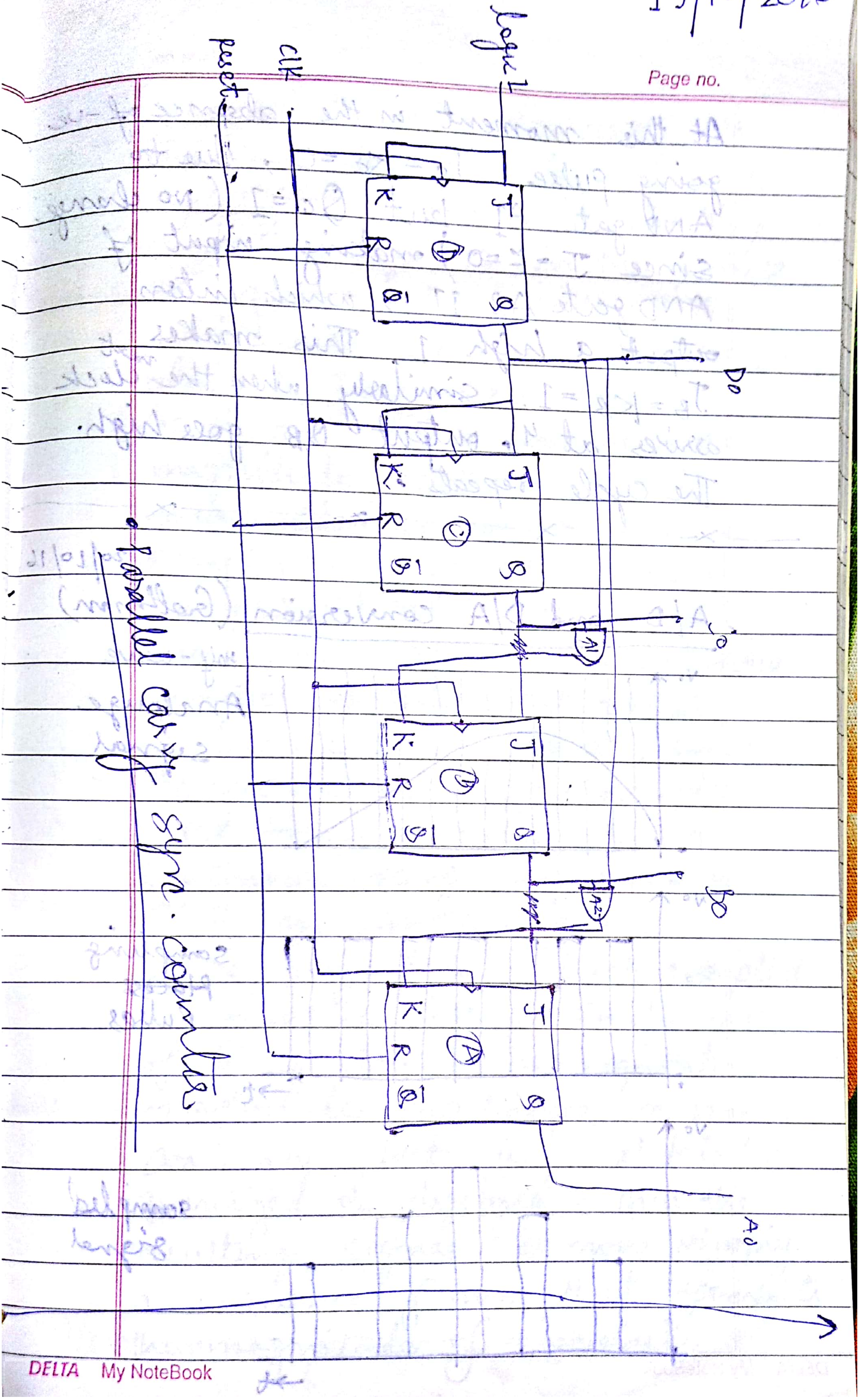
Scanned by CamScanner

are at zero.
At the arrival of first -ve going pulse at one the flip flop D toggles, since $J_D = K_D = 1$.
The output Q_D goes from low to High. It remain high till the next -ve going pulse that is at 2 with all the other flip flop remain zero.
As soon as Q_D goes high the input of the AND gate A1' become 1, 1. The AND gates outputs a high making a input of 'C' flipflop. $J_C = K_C = 1$. But the output Q_C remain low since the clockpulse is already at one '1'. At the arrival of next clock pulse at '2'. The flip flop D & C both toggled (Because both their inputs are high). The output Q_D changes from high to low whereas the ouput Q_C changes from low to high. Q_D remain low till 3. whereas the output Q_C remain high 4.



19/10/2016

Page no.



DELTA My NoteBook

Scanned by Imran Khalid

At this moment in the absence of -ve going pulse $J_c = K_c = 0$, due to AND gate A1 but $Q_c = 1$ (no change since $J - K = 0$) making input of AND gate A2 1, which intern output a high 1. This makes $J_B = K_B = 1$. similarly when the next clock arrives at 4, output Q_B goes high. The cycle repeats.

× × × ×

20/10/16

A/D and D/A conversion (Gothman)

Half-wave Analouge signal

Vo

sampling Pulses

Vo

sampled signal

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

Page no.

What is Sampling & Quantization.

→ The conversion of analog signal to digital form depend upon sampling and Quantization. In this process an analog signal voltage is divided into equal intervals along the time axis. At each of these time instance the magnitude of the signal is measured (they are known as samples and process is known as sampling.) The sampled signal no longer remain a continous function of time but rather a descrete time signal. Since the magnitude of each sample and take any values in a continous range, the signal is still an analog signal.

- If the magnitude of each sampled is converted into a finite no. of digits then the signal magnitude no longer remain continous but is said to be quantized or digitized. Thus the resulting signal is now simply a sequence of no. that represents the magnitudes of samples.

Scanned by Imran Khalid

24/10/16

Page no.

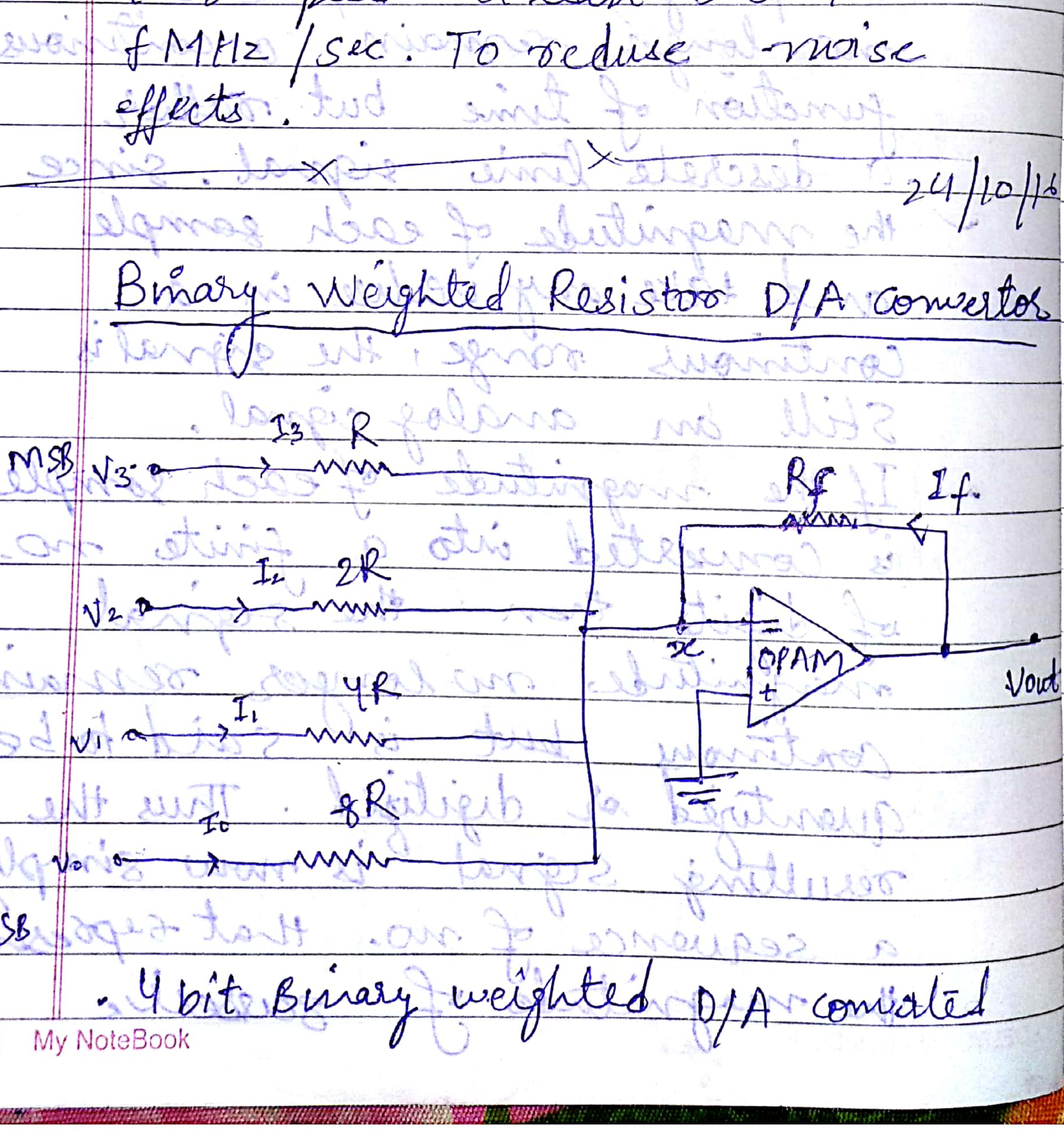
signal sampled:-

Nyquist Sampling theorem

If the highest frequency containg in an input analog signal is fm Hertz (1 KHz) then the input signal can be recovered with distortions if it is sampled at the rate of atleast two fm Hertz (2 KHz). However in practise it is necessary to sampled at least 5 to 10 fMHz/sec. To reduse noise effects.

24/10/16

Binary Weighted Resistor D/A convertor



- 4 bit Binary weighted D/A convated

Scanned by Imran Khalid

x = summing point (virtual ground)

OPAM = Operational Amplifier.

It consist of OP-amp. used as summing amplifier with binary weighted registers R, 2R, 4R, 8R. As shown in the figure the register R is MSB and 8R is LSB. The point x is summing point. V_3, V_2, V_1, V_0 are the inputs whose values can be logic 1 or 0. Whenever an input is logic 1 it will cost a current to flow in the register. When the input is logic 0 no current will flow in the registers. The OPAM adds the current flowing in each register at point x. This current flows in the feedback register Rf to produce a voltage V_1. The magnitude of output voltage is ∝ to the total current flowing Rf and hence with the input digital word.

Scanned by Imran Khalid

Apply KCL at point x,

$$I_3 + I_2 + I_1 + I_0 = -I_f \quad \text{— (i)}$$

$$= \frac{V_3}{R} + \frac{V_2}{2R} + \frac{V_1}{4R} + \frac{V_0}{8R} = -\frac{V_{out}}{R_f} \quad \text{— (ii)}$$

The eq(i) indicates that the summing amplifier passes the complete signal at V_3. But V_2, V_1 & V_0 it reduces by 1/2, 1/4, 1/8 respectively. Thus we can say the output summing amplifier is an analog voltage which represents the weighted sum of the digital input signal. The -ve sign in the output shows the amplifier is used as ~~converting~~ inverting amplifier. Let the input of the D/A be 1001. Let the voltage level be 5V for logic 1. Let $R = 10\,K\Omega$, $R_f = 5K\Omega$ then the current will flow in register R and 8R and no current will flow in register 2R and 4R. The magnitude of current will be $I_3 = \frac{5}{(10 \times 10^3)} = 0.5\ mA$,

Scanned by Imran Khalid

$I_0 = \frac{5V}{(8 \times 10 \times 10^3)} = 0.0625\ mA$

and $I_1 = I_2 = 0\ mA$

The total current flowing in the OPAM will be $0.5 + 0.0625 = 0.5625\ mA$. The output voltage will be $= 0.5625 \times 5 \times 10^3 = 2.8125\ V$.

The conversion accuracy of this D/A converter will depend upon two factors.

(1). The precision of the input and feedback register.

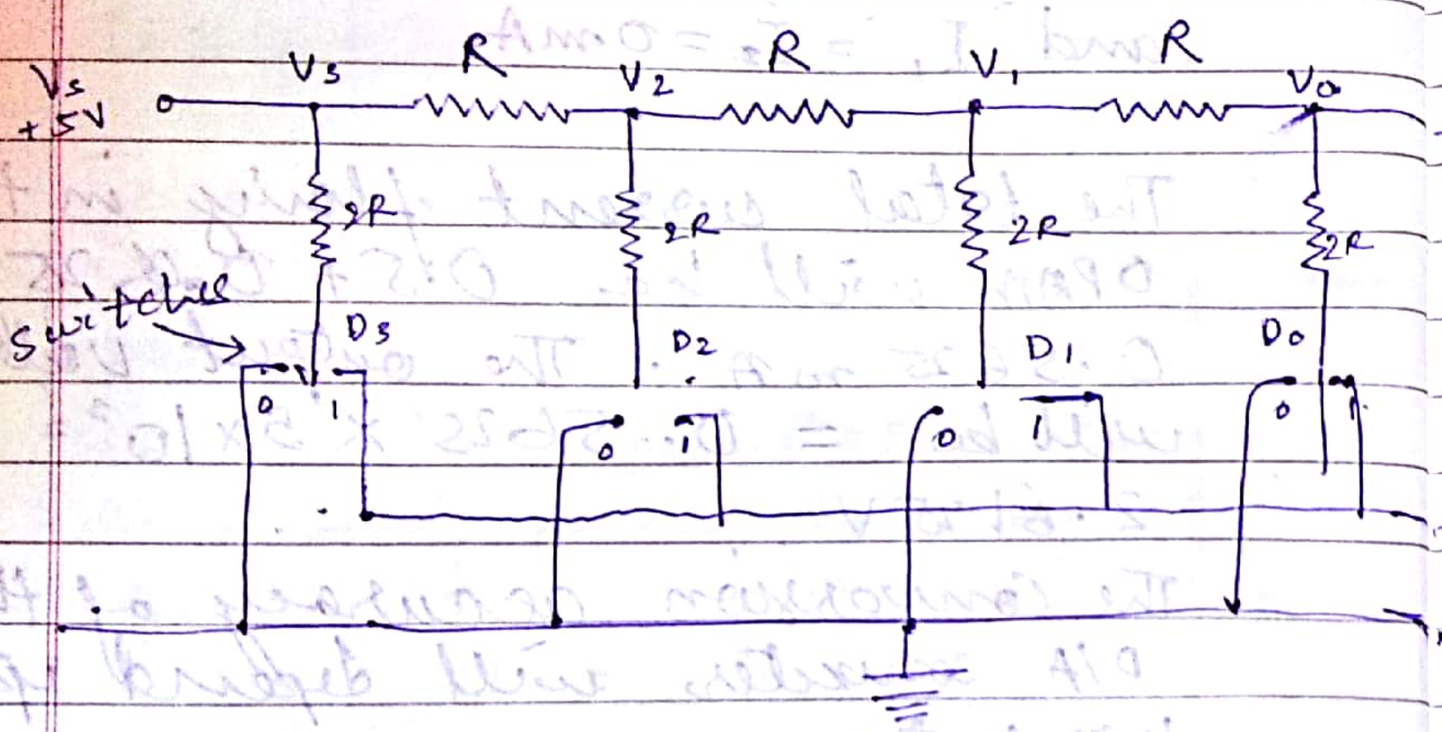
(2) The precision of the input voltage levels.

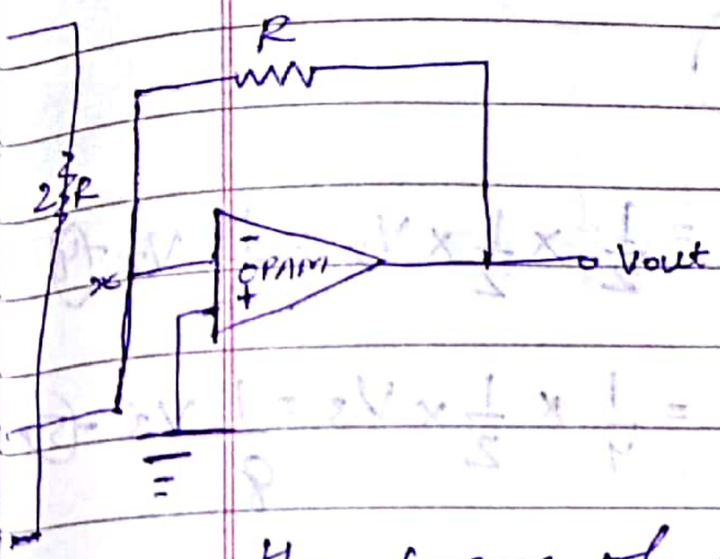
(3) The precision of the registers can be made by using high quality registers such as metal film or Oxide film registers. since the output of flip flop or logic gates do not always produce precise value of 0 & 5 V, semiconductor switches connected to a reference voltage to utilized to provide logic 0 & 1.

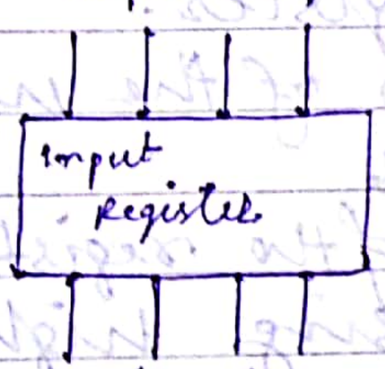
DELTA My NoteBook

Scanned by CamScanner

D/A Converter – R/2R or ladder network







$$V_2 = \frac{R_2}{R_1+R_2} \times V$$

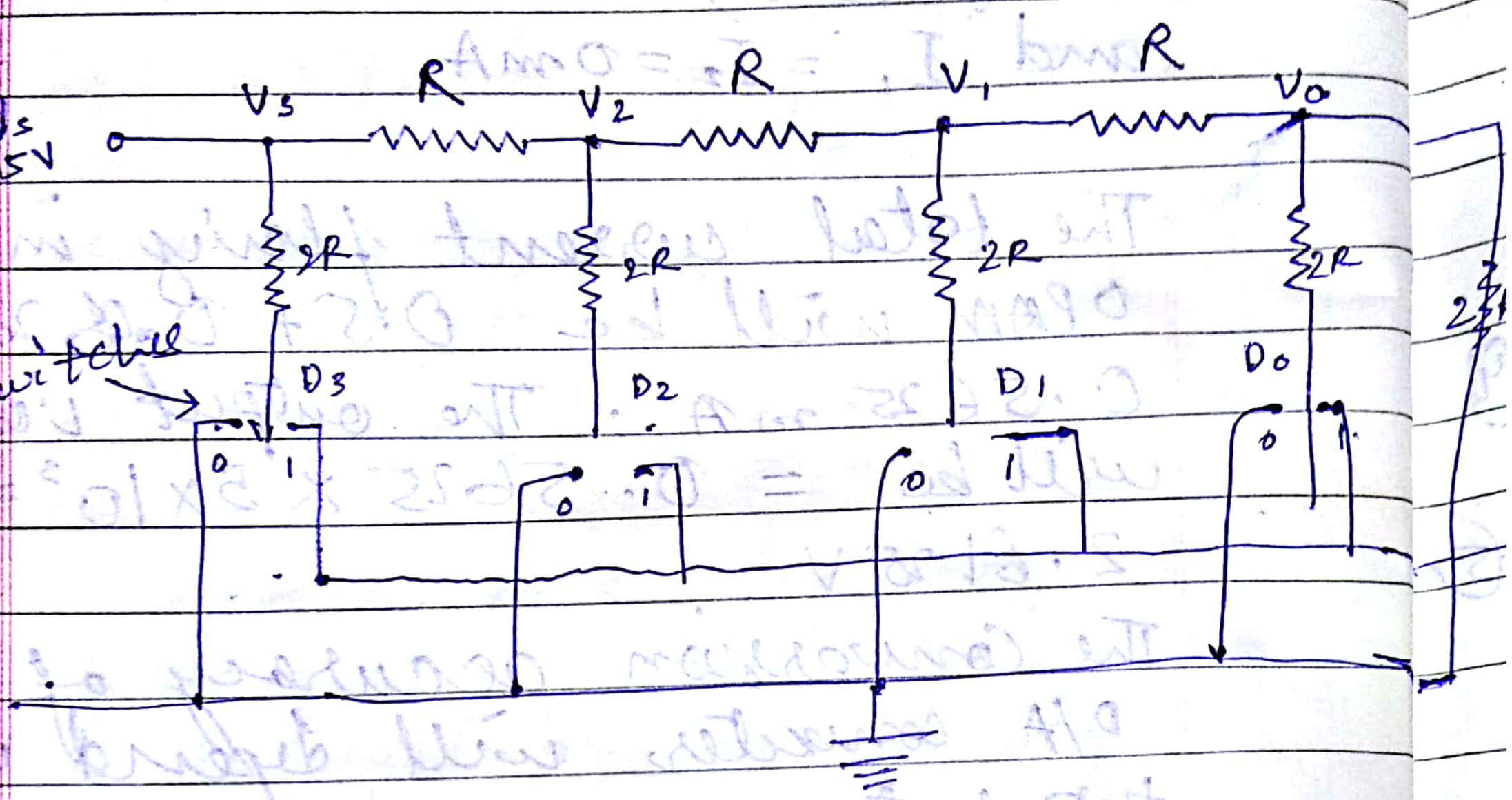
To overcome the drawback of weighted register network, the ladder network is used as shown in the figure.
It uses only 2 precision resistors having values of R & 2R in the form of a ladder.
The input to DAC is determine from shift registers. The four bit binary no. is represented by D_0, D_1, D_2, D_3 where D_0 LSB and D_3 MSB. Also each bit control a switch between ground and inverting input of OPAM. IN the ladder network the output is based upon the principle of superposition.

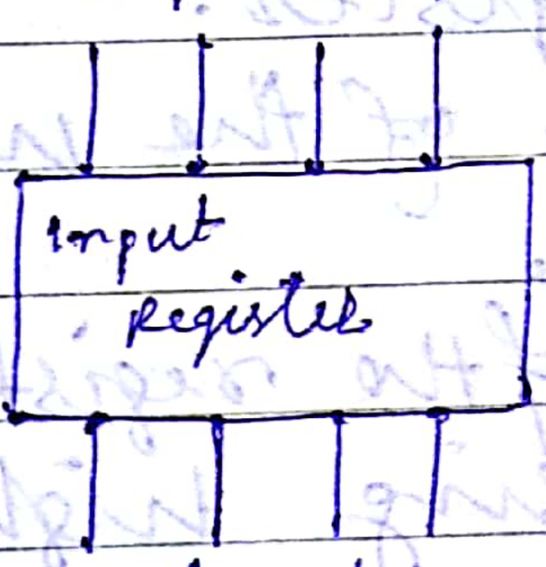
0001
0010
0100
1000

be the input.

Scanned by Imran Khalid

D/A Converter — R/2R or ladder network



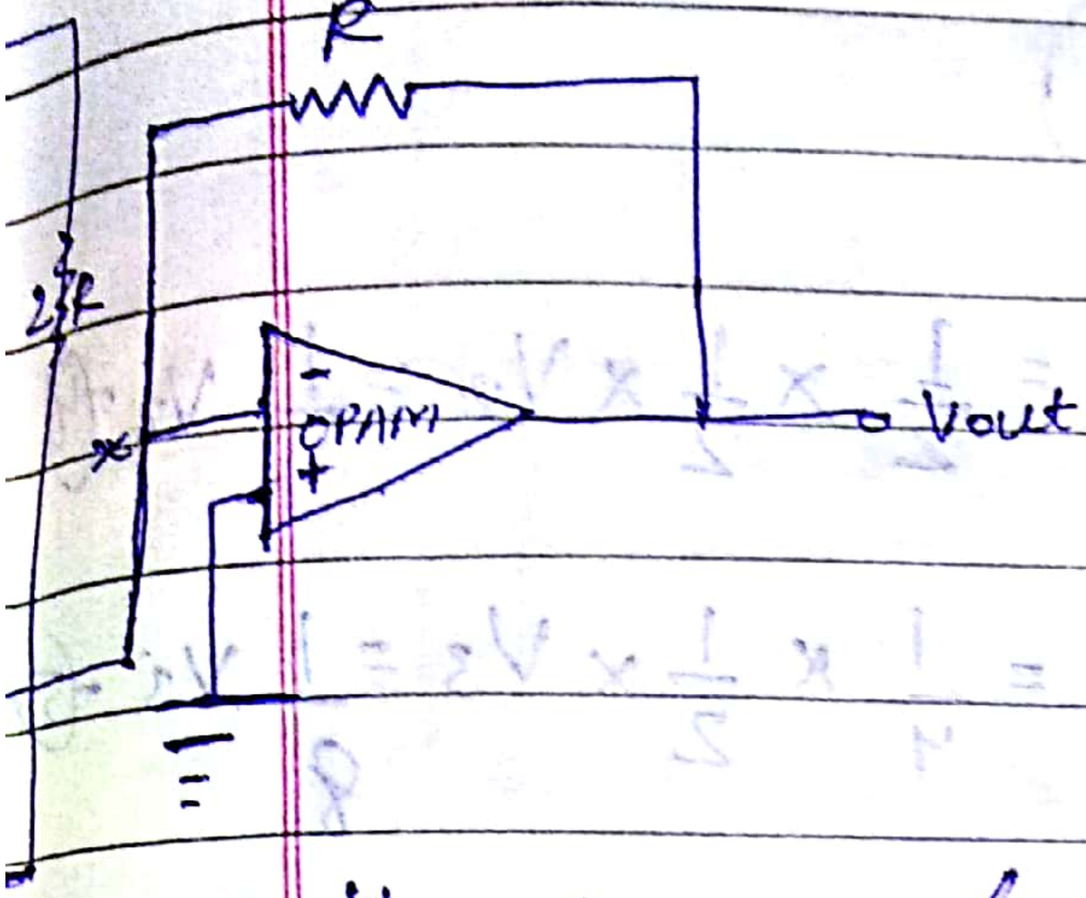


$$V_L = \frac{R_2}{R_1 + R_2} \times V$$

To overcome the drawback of weighted register network, the ladder network is used as shown in the figure.
It uses only 2 precision registors having values of R & 2R in

DELTA My NoteBook

Scanned by Imran Khalid



the form of a ladder.
The input to DAC is determine from shift registers. The four bit binary no. is represented by D_0, D_1, D_2, D_3 wher D_0 LSB and D_3 MSB. Also each bit control a switch between ground and inverting input of OPAM. IN the ladder network the output is based upon the principle of superposition.

0001
0010
0100
1000
be the input.

Scanned by Imran Khalid

$$V_0 = \frac{1}{2} V_1 \quad \text{— (i)}$$

$$V_1 = \frac{1}{2} V_2 \quad \text{— (ii)}$$

$$V_2 = \frac{1}{2} V_3 \quad \text{— (iii)}$$

From (i), (ii) $V_0 = \frac{1}{2} \times \frac{1}{2} \times V_2 = \frac{1}{4} V_2$ — (4)

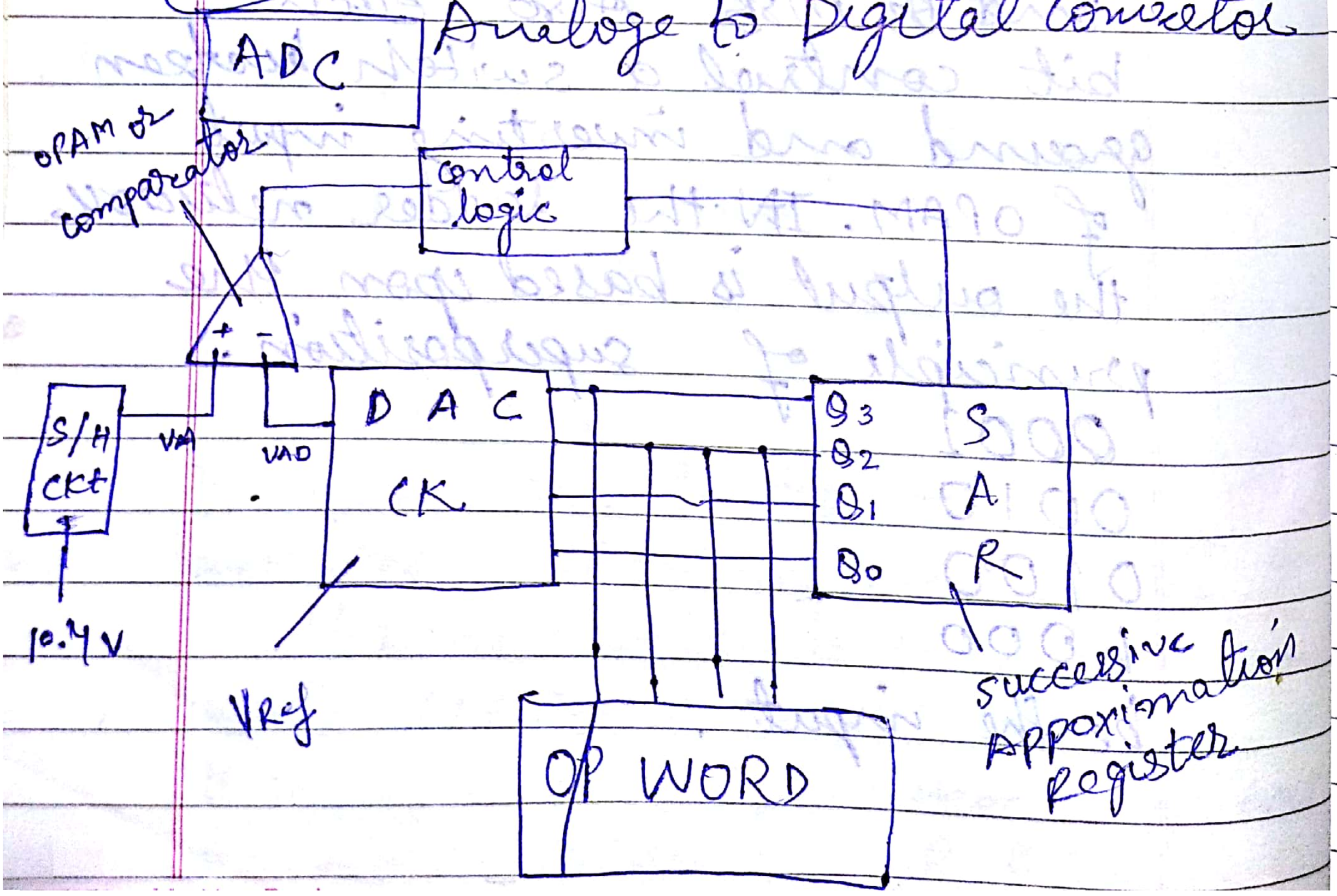
from (3) & (iv), $V_0 = \frac{1}{4} \times \frac{1}{2} \times V_3 = \frac{1}{8} V_3$ — (5)

Some $V_3 = V_S$

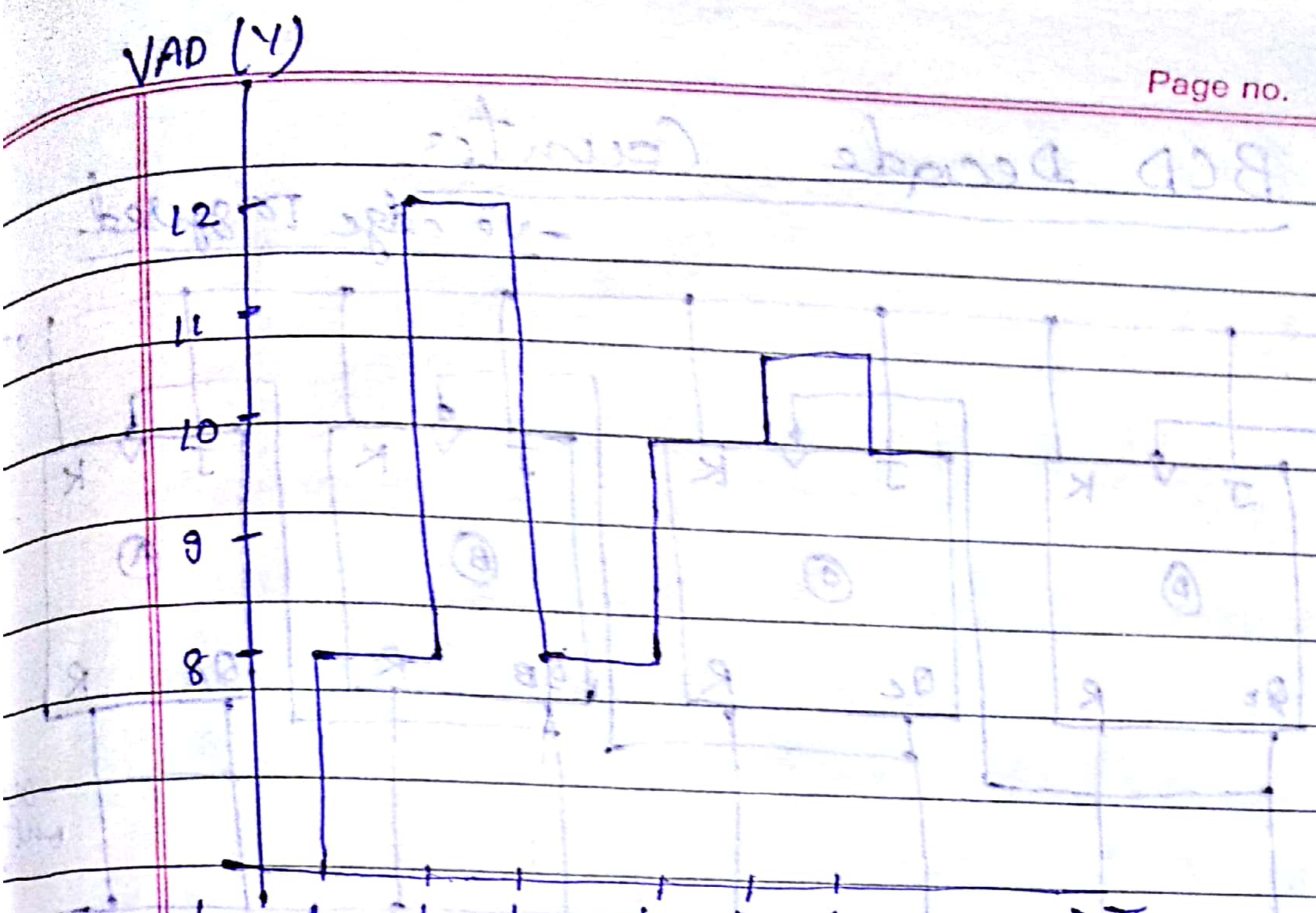
$$V_0 = \frac{1}{8} V_S \quad \text{— (6)}$$

26/10/2016

Successive Approximation Analoge to Digital convertor



Scanned by Imran Khalid



• Timing Diagram.

0	0	0	0	0	
1	0	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	1	1	1	0	
5	0	0	1	0	
6	0	0	0	1	
7	1	0	0	1	
8	0	1	0	1	
9	0	1	1	0	

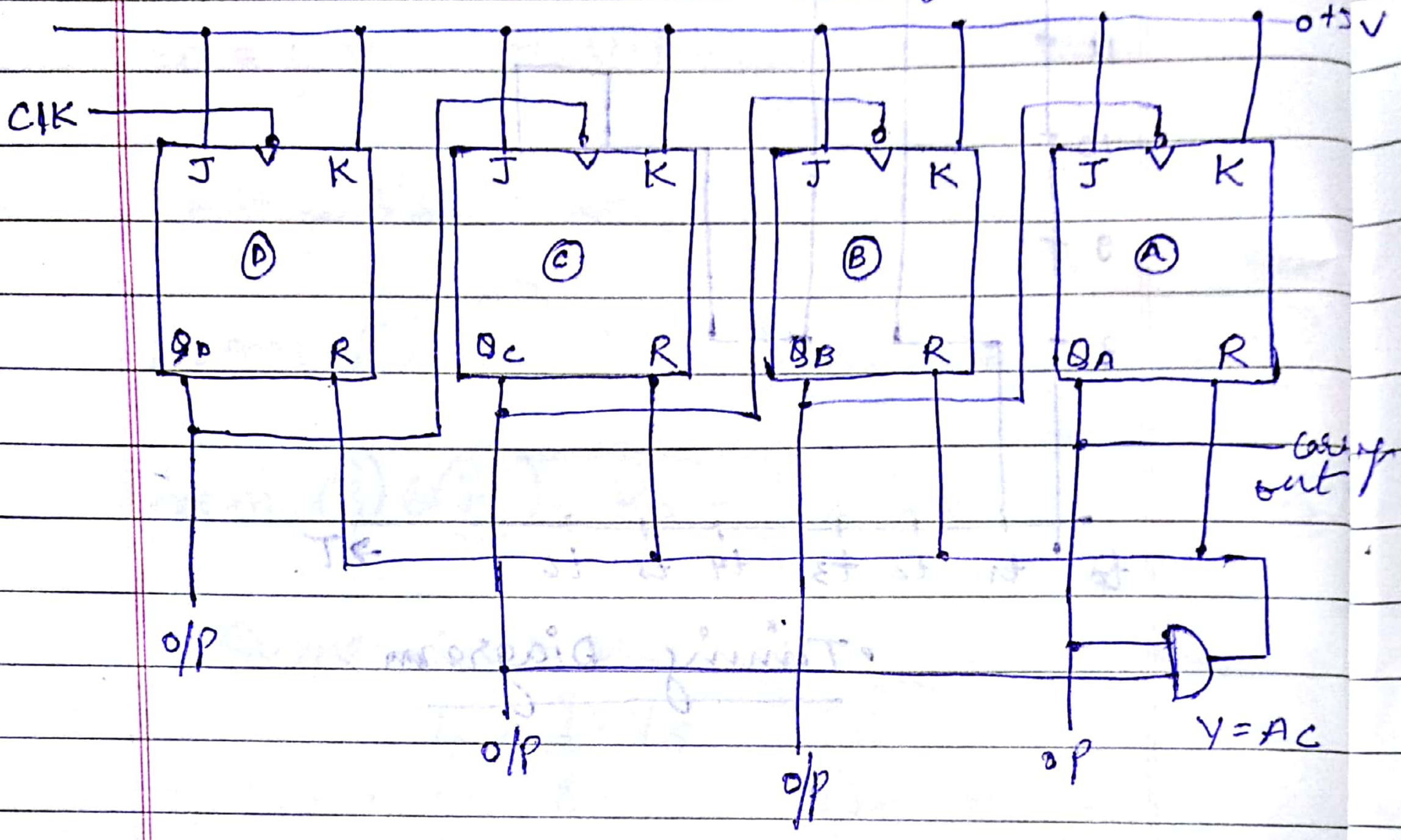
Scanned by Imran Khalid

31/10/2016

Page no.

BCD Decade Counter

-ve edge triggered.



Q_A	Q_B	Q_C	Q_D	Dec.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	R

Scanned by Imran Khalid

Page no.

It is a normally counts decimal digits from 0 to 9 and then reset itself. At the end of the ninth count a carry is generated which is used for the BCD count of the next decimal digit.

The interconnection between successive flip flop follow the normal ripple sequence starting with the initial state as $Q_A = Q_B = Q_C = Q_D = 0$ till the count of 9. The output of the counter can be read directly in BCD code. During the interval when the counter goes from 9 to 0, a -ve going signal edge occurs at the carry output which is connected to the input of another BCD counter.

DELTA My NoteBook

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

01/11/2016

Page no.

Resolution

It is defined as the smallest possible change in the output analog voltage due to the change in digital input.

The resolution is always equal to weight of LSE and is also known as stepped size.

The resolution of 'n'-bit DAC using weighted register and ladder network is given as 2^n volts usually resolution is expressed as % resolution given as $1/2^{n-1} \cdot 100$.

Q→ Find the resolution & % resolution for a five bit ladder network if the binary ladder has a full scale of 10 volt. maximum output $\frac{V_{max}}{2^n}$.

Sol=. Resolution $\frac{V_{max}}{2^n} = \frac{10}{(2)^5} = \frac{10}{32} = .3125$ V

This pdf file is downloaded from http://www.diplomacs.com

Scanned by Imran Khalid

(That is output changes in steps of 0.3125 volts).

∴ Resolution = 31.25 % - 1

= 6.25 V

% Resolution → $\frac{1}{2^n} \times 100$

where, n = bit ladder.

Don't misuse this E-note.

Contributor- IMRAN KHALID
This pdf is downloaded from www.diplomacs.com

www.imrankhalid.in

Note:For any illegal use of this pdf file only the user will be responsible, not the owner or the contributor !

Scanned by Imran Khalid